PIE Tech

POLLACHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Approved by **AICTE** and Affiliated to **Anna University**)

sky is the limit

Department of Electrical and Electronics Engineering

Regulation 2021

II Year – IV Semester

EC3402- Linear Integrated Circuits

EE 8451 LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

UNIT . I IC FABRICATION :

IC classification, fundamental of monolithic IC technology, epitaxial growth, masking and etching, diffusion of impurities, Realisation of monolithic ICs and packaging. Fabrication of diodes, capacitance, resistance, FETs and PV cell.

Introduction :-

The integrated circuit or IC is a miniature low cost, electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon.

Advantages :-

1) Miniaturization and hence increased equipment density.
2) Cost reduction due to batch processing.
3) Increased system reliability due to elimination of soldered joints.
4) Improved functional performance.
5) Matched devices.
6) Increased operating speeds.
7) Reduction in power consumption.

classification :-

i) Digital Ics.

ii) Linear Ics.

⇒ Two different Ic Technologies namely,

1) Monolithic Technologies.

2) Hybrid Technologies.

Monolithic Technology :-

All circuit components, both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon.

Suitable for identical circuits are required in very large quantities and hence provides lowest per-unit cost and highest order of reliability.

Hybrid Technology :-

Separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bonds. More suitable for small quantity custom circuits.

Based upon active devices, Ics classified as

Bipolar (using BJT)

unipolar (using FET).

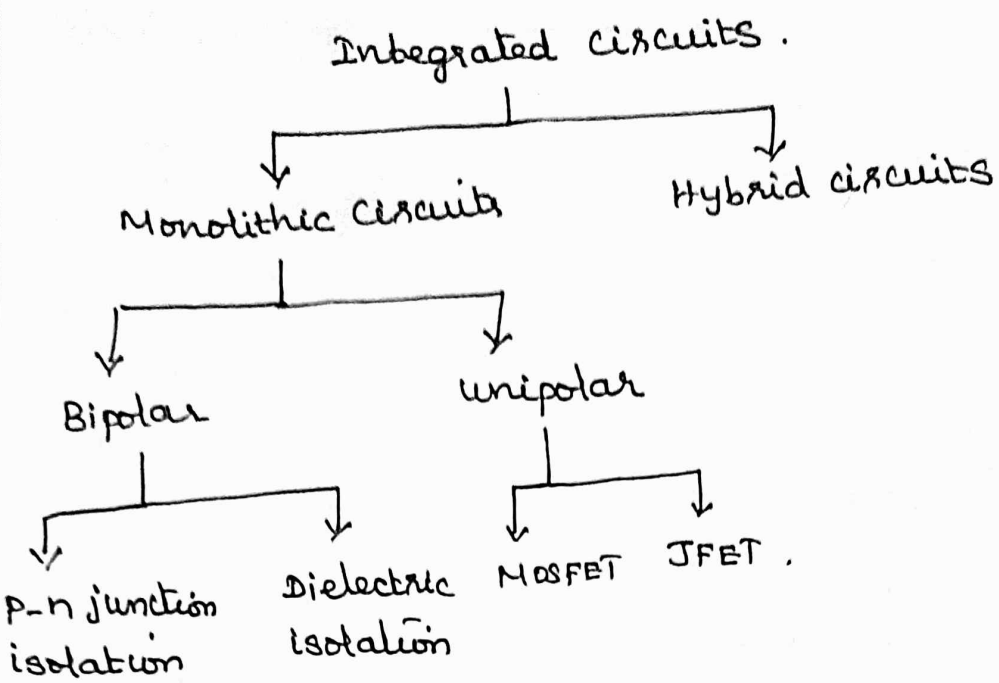


Fig : classification of ICs.

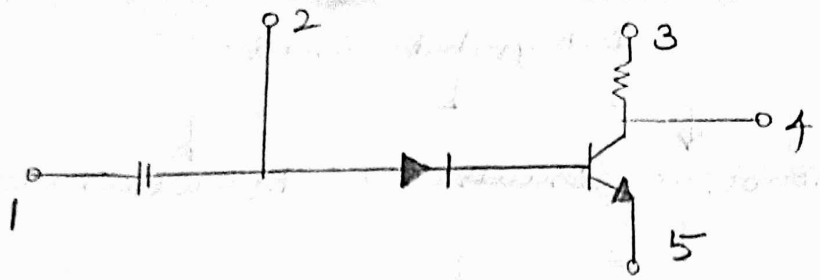
Fundamentals of Monolithic IC Technology :-

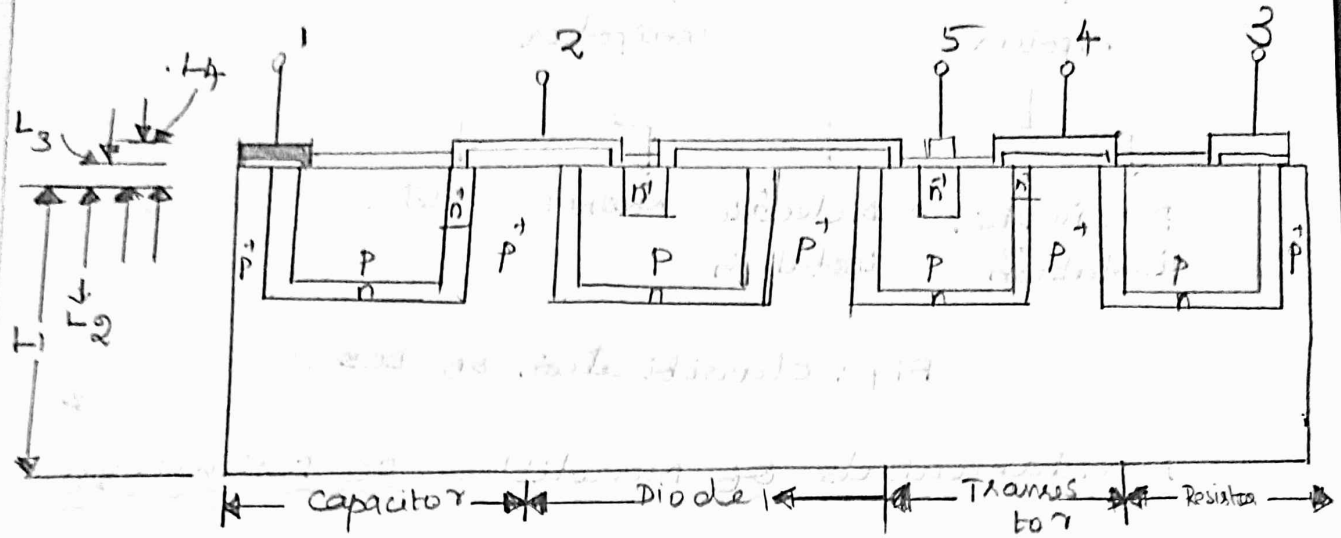
Monolithic → Greek word.

Monolithic Integrated circuits are made in a single piece of single crystal silicon.

A standard 10 cm diameter wafer can be divided into approximately 8000 rectangular chips of sides 1 mm. Each IC chip may contain as few as tens of components to several thousands components. And if 10 such wafers are processed in one batch, we can make 80,000 ICs simultaneously.

Many chips produced will be faulty due to imperfection in the manufacturing process. Only 16,000 good chips are produced in a single batch.





Layer NO : 1 (~400μm) : is a p-type silicon substrate upon which the integrated circuit is fabricated.

Layer NO : 2 (5-25μm) : is a thin n-type material growth as a single crystal extension of the substrate using epitaxial deposition technique. All active and passive components are fabricated within this layer using selective diffusion of impurities

Layer NO : 3 (0.02 - 2μm) : is a very thin SiO_2 layer for preventing diffusion of impurities wherever not required using photolithographic Technique

Layer NO : 4 (1μm) : is an aluminium layer used for obtaining interconnection between components.

Basic Planar Processes :-

The basic processes used to fabricate ICs using silicon planar Technology can be follows :

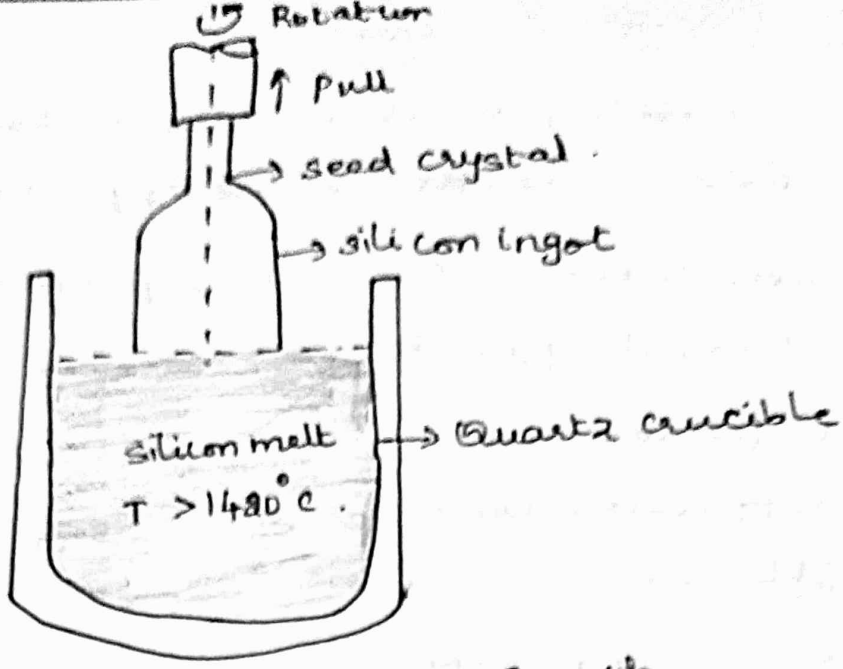
1. silicon waber (substrate) preparation
2. Epitaxial growth
3. Oxidation
4. Photolithography
5. Diffusion
6. Ion implantation
7. Isolation Technique
8. Metallization
9. Assembly processing and packaging

1) Silicon waber preparation :

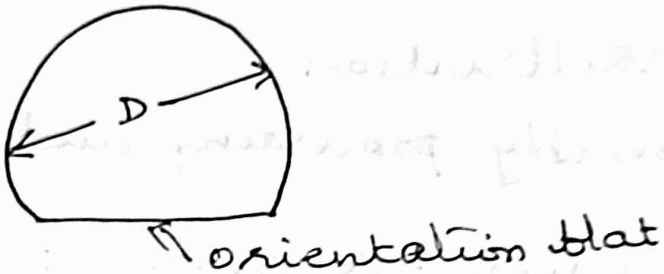
The following steps are used in preparation of si-wabers :

1. crystal growth and doping
2. Ingot trimming and grinding
3. Ingot slicing
4. waber polishing and etching
5. waber cleaning.

Czochralski crystal Growth process : It is often used for producing single crystal silicon ingots. The ~~poly~~ highly purified (99.9999) Polycrystalline silicon together with an dopant is put in a quartz crucible and then placed in a furnace.



Czochralski crystal Growth.



Silicon waber, D = 10, 18.5, 15 cm
showing flat orientation

=> The material is then heated to a temperature of 1420°C.

=> A small single crystal rod of silicon called seed crystal is dipped into the silicon melt and slowly pulled out. It brings solidified mass of silicon with the same crystalline structure as that of seed crystal.

=> During the process, the seed crystal and the crucible are rotated in opposite directions in order to produce ingots of circular cross section. Ingot diameter 10 to 15 cm, length 100cm

=> The top and bottom portions of the ingot are cut-off and the ingot surface is ground to produce an exact diameter CD = 10, 12.5, 15 cm

=> The ingot is sliced using a stainless steel saw blade with industrial diamonds embedded into the inner diameter cutting edge. This produces circular wafers or slices.

=> The orientation flat portion serves as a useful reference plane.

=> The obtained silicon wafers undergo a number of polishing steps to produce a flat surface.

=> After all the IC fabrication processes are complete then wafers are sawed into 100 to 8000 rectangular chips having side of 10 to 1mm. Each chip is

a single IC and contain hundreds of components.

(4) EPITAXIAL GROWTH :

Epitaxy means, arranging atoms in single crystal fashion upon a single crystal substrate, so resulting layer is an extension of the substrate crystal structure.

⇒ The process is carried out in a reaction chamber consisting of a long cylindrical Quartz tube encircled by an RF induction coil.

⇒ The silicon wafers are placed on a rectangular graphite rod called a boat.

⇒ This boat is then placed in the reaction chamber where the graphite is heated inductively to a temperature 1200°C.

⇒ Various gases required for the growth of desired epitaxial layers are introduced into the system through a control console.

$$SiCl_4 + 2H_2 \underset{}{\overset{1200^\circ C}{\rightleftharpoons}} Si + 4HCl$$

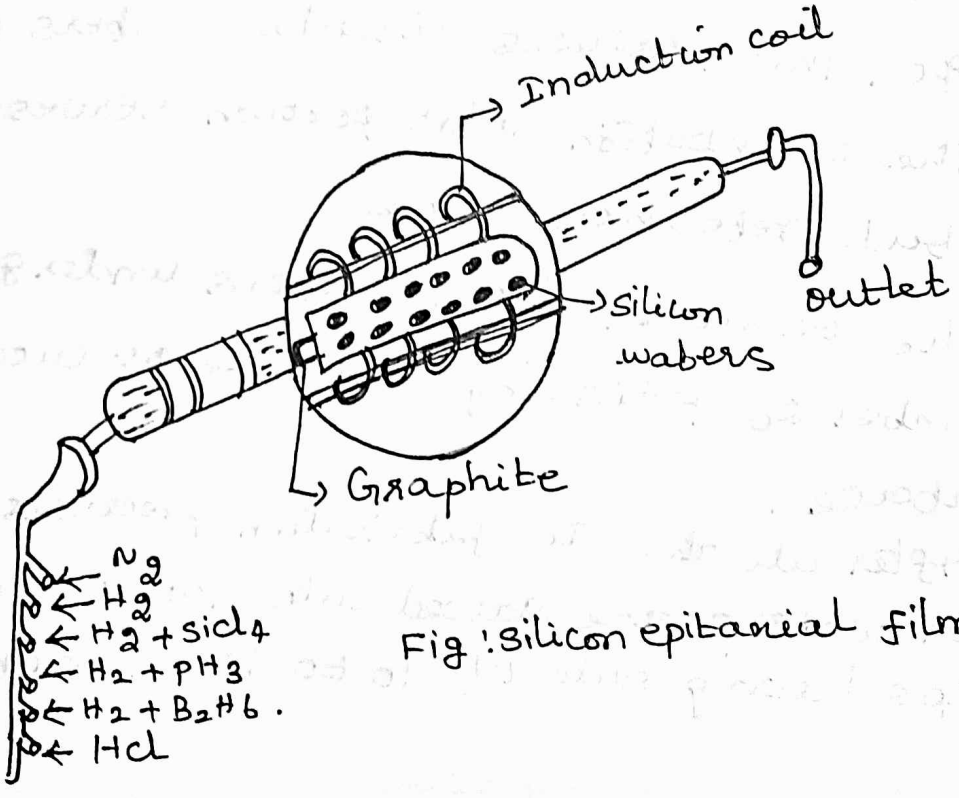


Fig : Silicon epitaxial films.

3) OXIDATION :- [Thermal oxidation]

SiO_2 has the property of preventing the diffusion of all impurities through it. It serves 2 purposes

i) SiO_2 is an extremely hard protective coating and unaffected by almost all reagents except hydrofluoric acid.

ii) By selective etching SiO_2, diffusion of impurities through carefully defined windows in the SiO_2 can be accomplished to fabricate various components.

Silicon wafers are stacked up in a Quartz boat and then inserted into Quartz furnace tube. The Si-wafers are raised to a high temperature in the range of 950 to 1115°C, and exposed to a gas containing O_2 or H_2O or both.

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2.$$

Thickness of oxide layer is 0.02 to 2μm.

4) Photolithography :-

photolithography is used to produce microscopically small circuit. It uses x-ray or electron beam lithographic techniques, to produce device dimensions down to sub-micron range (<1 μm).

It involves two processes

1) Making of a photographic mask,

2) Photo etching.

(i) Making of a photographic Mask :-

Involves the following sequence of operations

i) Initial artwork.

ii) Reduction.

Initial artwork is done at a scale several hundred times larger than the final dimensions of the finished monolithic circuit. Drawings are made magnified and often by a factor of 500. The width of one mil is magnified to a width of 500 mils, i.e 1.8 cm. So, finished monolithic chip of area 50mil x 50mil, the artwork will be made on an area of about 60cm x 60cm.

The artwork should not contain any line drawings but alternate clear and opaque regions. This is accomplished by the use of clear Mylar coated with a sheet of red photographically opaque mylar (Rubylith). Artwork is produced on a precision drafting machine known as coordinatograph.

This rubylith pattern of individual mask is photographed and then reduced in steps by a factor of 5 or 10 several times to finally obtain the exact image size. The final image repeated many times in a matrix array so that many ICs will be produced in one device process.

The photo repeating is done with a step and repeat camera. This is an imaging device with a photographic plate on a movable platform. Between exposure the plate is moved in equal steps so that successive images form in an array.

When the exposed plate is developed, it becomes a master mask.

Photo-etching :-

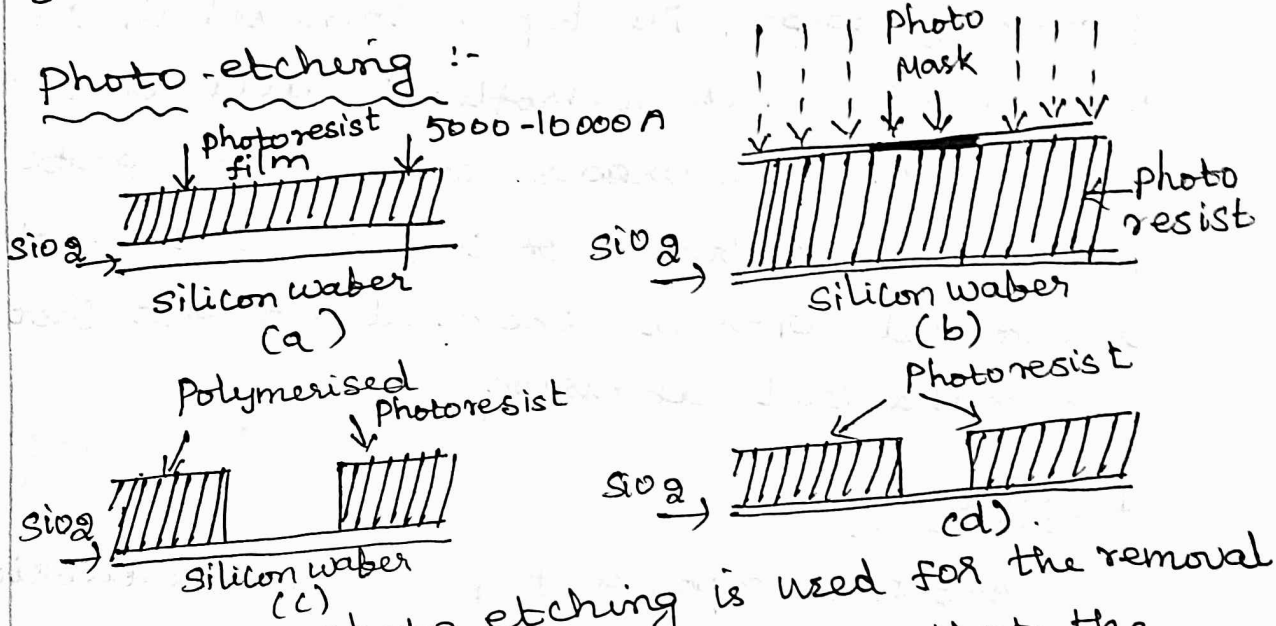


photo etching is used for the removal of SiO_2 from desired regions, so that the desired impurities can be diffused. The waber is coated with a film of photosensitive emulsion (Kodak photoresist KPR). The thickness of the film is in the range of 5000-10000A

The mask negative of the desired pattern prepared by steps earlier is placed over the photoresist coated waber. This is now exposed to ultraviolet light, so that the KPR becomes polymerized beneath the transparent regions of the mask.

The mask is then removed and the wafer is developed using a chemical (trichloroethylene) which dissolves the unexposed / unpolymerized regions on the photoresist and leaves the pattern fig (c).

The polymerised photoresist is next fired or cured, so that it becomes immune to certain chemicals called etchants used in subsequent processing steps. The chip is immersed in the etching solution of hydrofluoric acid, which removes the SiO_2 from the areas which are not protected by KPR. After diffusion of impurities, the photoresist is removed with a chemical solvent (hot H_2SO_4) and mechanical abrasion.

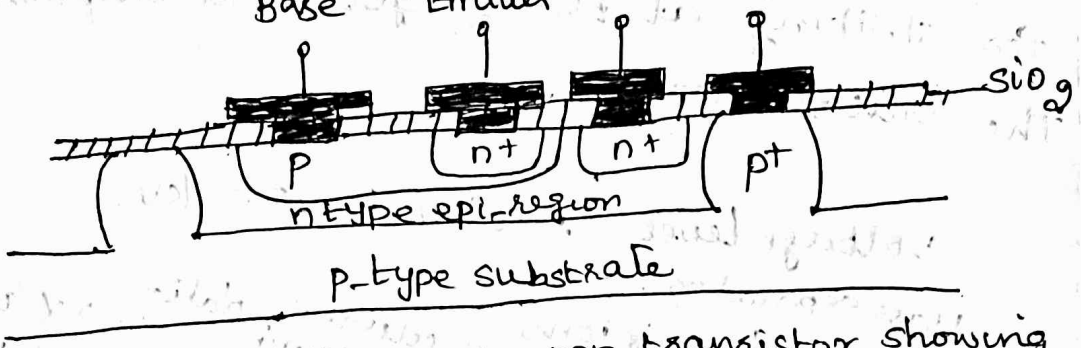
Diffusion :-

Another important process in the fabrication of monolithic ICs is the diffusion of impurities in the silicon chip. This uses a high temperature furnace having a flat temperature profile over a useful length (about 20" length).

A quartz boat containing about 20 cleaned wafers is pushed into the hot zone with temp maintained at about a 1000°C.

Components such as B_2O_3 (Boron Oxide), BCl_3 (Boron chloride) are used for Boron and P_2O_5 (Phosphorous pentaoxide) and $POCl_3$ (phosphorous oxychloride) are used as sources of Phosphorous.

A carrier gas such as dry oxygen or nitrogen is normally used for sweeping the impurity to the high temperature zone. The depth of diffusion depends upon the time of diffusion which normally extends to 2 hours.



Cross section of an npn transistor showing curved junction profiles as a result of lateral diffusion.

Ion Implantation :-

⇒ This technique used to introduce impurities into a silicon wafer.

⇒ It is the process, the ions of a particular impurity or dopant material are accelerated by an electric field to a very high velocity and lodge the dopant within the semiconductor material.

⇒ A gas containing the desired impurity is ionized inside an ion source.

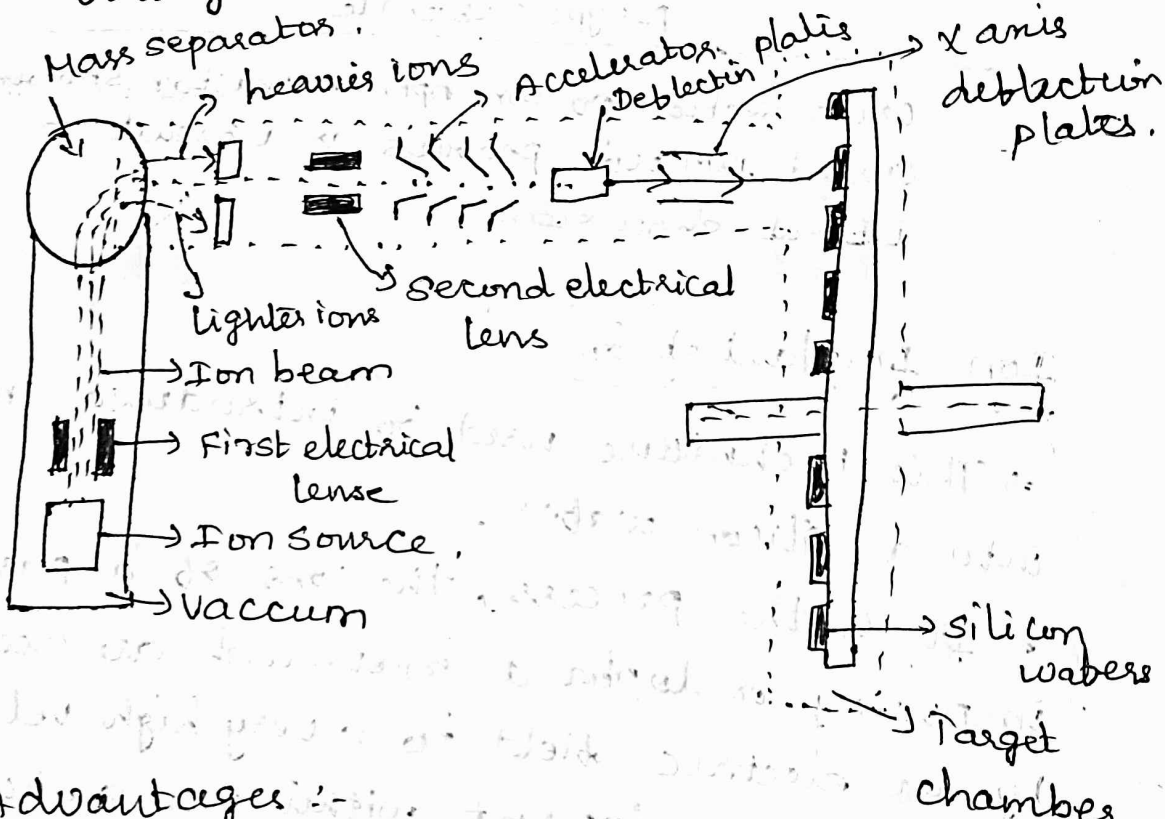
⇒ The ions are generated and directed from the source in a diverging beam and focussed. Then pass through a mass separator.

⇒ Mass separator directs only the ions of the desired dopant.

⇒ Second lens focuses this beam, then passed through an accelerator.

⇒ Accelerator imparts the required energy for striking at the target and implanted in the silicon wafer.

Voltage level : 20KV to 250 KV.



Advantages :-

1) Accurate control over doping
2) Very good reproducibility.
3) Room temp process.

Limitations :-

1) Higher temperature is required for avoid the crystal damage.
2) Possibility of dopant implanting through various layers of wafers.

Assembly Procesing and Packaging :-

Each of the waber procesed contains several hundred chips, each being a complete circuit. so these chips must be separated and individually Packaged. A common methed called scribing and cleaving used for separation makes use of a diamond tipped tool to cut lines into the surface of the water along the rectangular grid separating the individual chips.

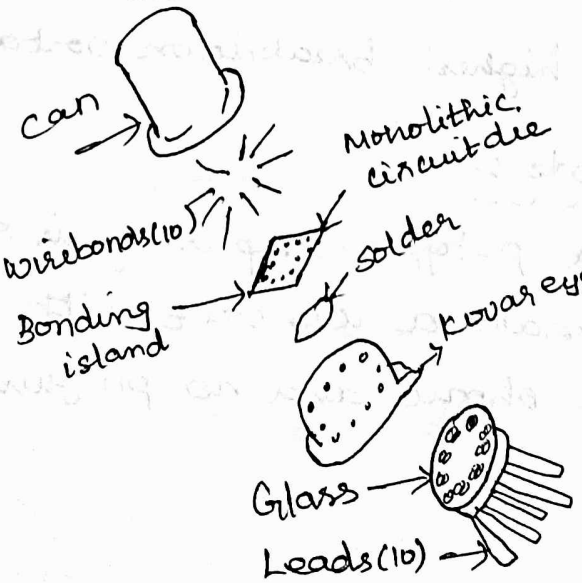
The waber is fractured along the scribe lines and the individual chips are phyically reparated. Each chip is then mounted on a ceramic waber and attached to a suitable package.

Three different package configurations are

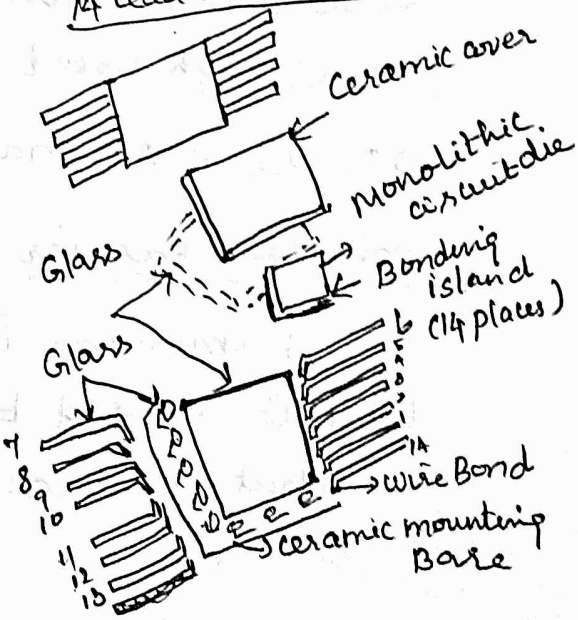
1) Metal can package - available in 8, 10, 12 leads.
2) ceramic flat package → costly due to fabrication process.
3) Dual-in-line (ceramic or plastic type) package.
   → 8, 14, 16 leads (or) 24 or 36 or 42 leads.

↳ Advantage : Best hermetic sealing.

TO-5 Metal package



14 Lead version of flat package

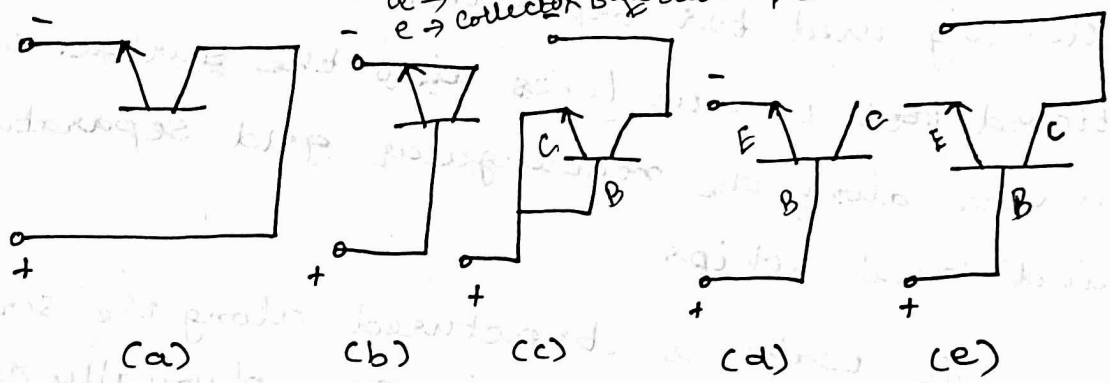


Fabrication of Diodes :-

Monolithic Diodes :-

Figure shows the five different possible connections by which a transistor could be utilized as a diode. c, d, e are popular.

c → emitter Base diode, collector short circuited to the base
d → emitter Base diode, collector open.
e → collector Base diode, emitter open circuited.



(a) (b) (c) (d) (e)

Cross section view of various diode structure.

characteristic	(a) $V_{CB}=0$	(b) $V_{CE}=0$	(c) $V_{EB}=0$	(d) $I_C=0$	(e) $I_E=0$
Breakdown voltage (volts)	7	7	55	7	55
storage time, (n sec)	9	100	53	56	85
Forward voltage (volts)	.85	.92	.94	.96	.95

⇒ The diode 'a' is useful for high speed, lowest storage time, lowest forward voltage drop.

⇒ diode b & d used for stored charge device and high speed turn-off of the transistor.

⇒ Diode c & e have highest breakdown voltage.

Schottky Barrier Diode :-

Aluminium is a p-type impurity in silicon. When it is fired to make a contact with n-type Si, that contact is ohmic and no pn junction is formed.

=> This is done by making n^+ diffusions in the n-regions near the surface where Al is deposited.

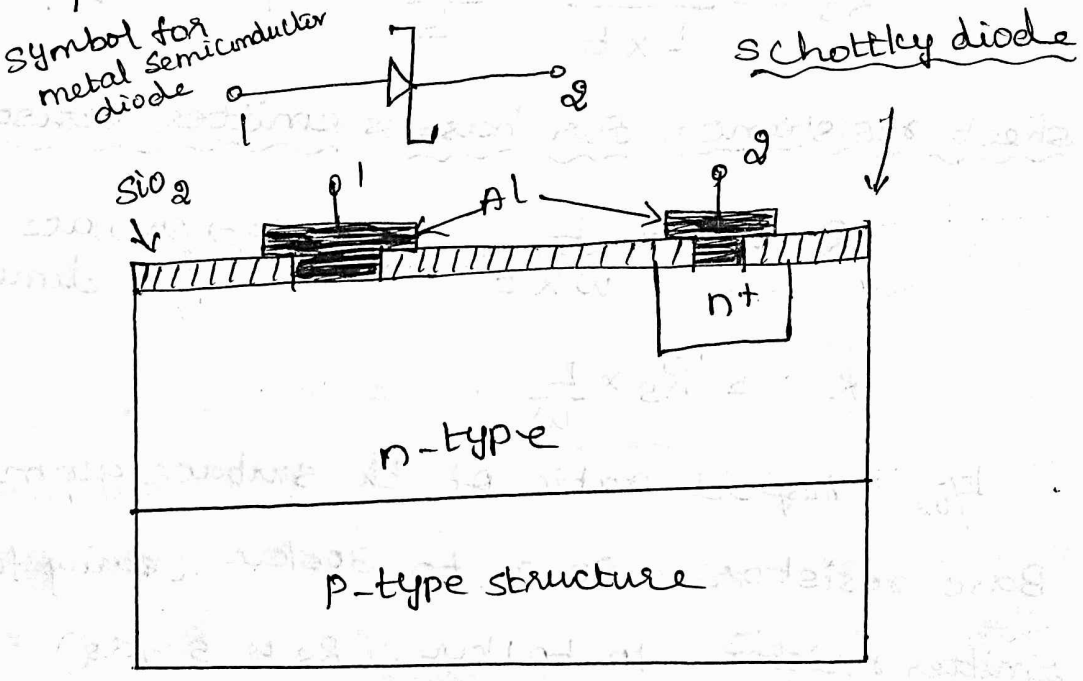
=> If Al is deposited directly upon the n-type Si, a metal semiconductor diode is formed.

=> Fig shows two contacts, Contact 1 is a schottky barrier and contact 2 is an ohmic contact.

=> The contact potential between the semiconductor and the metal creates a barrier to the flow of conduction electrons from semiconductor to metal.

=> Forward biasing the junction lowers this barrier and permit electron flow from semiconductor to metal where electrons are abundant. Majority carrier electrons carry current in a schottky diode.

=> Schottky diodes has less forward voltage (0.3V) compared to the PN diode ($V_\gamma = 0.6V$).



Symbol for

Integrated Resistor : (Fabrication of R)

4 different methods

1) Diffused Resistor
2) Epitaxial Resistor
3) Pinched Resistor
4) Thin film Resistor.

Diffused Resistor :-

Resistor is formed in one of the isolated regions of epitaxial layer during base or emitter diffusion, common to bipolar transistor fabrication. Small range of resistances possible.

Sheet Resistance (R_S) :-

Consider the square L x L of a material, resistivity ρ, thickness t, Cross sectional Area A

$A = L \times t$. Resistance of this sheet of material

$$R_S = \frac{\rho L}{L \times t} = \frac{\rho}{t} \quad (\Omega/\text{square}).$$

Sheet resistance for base & emitter resistor :-

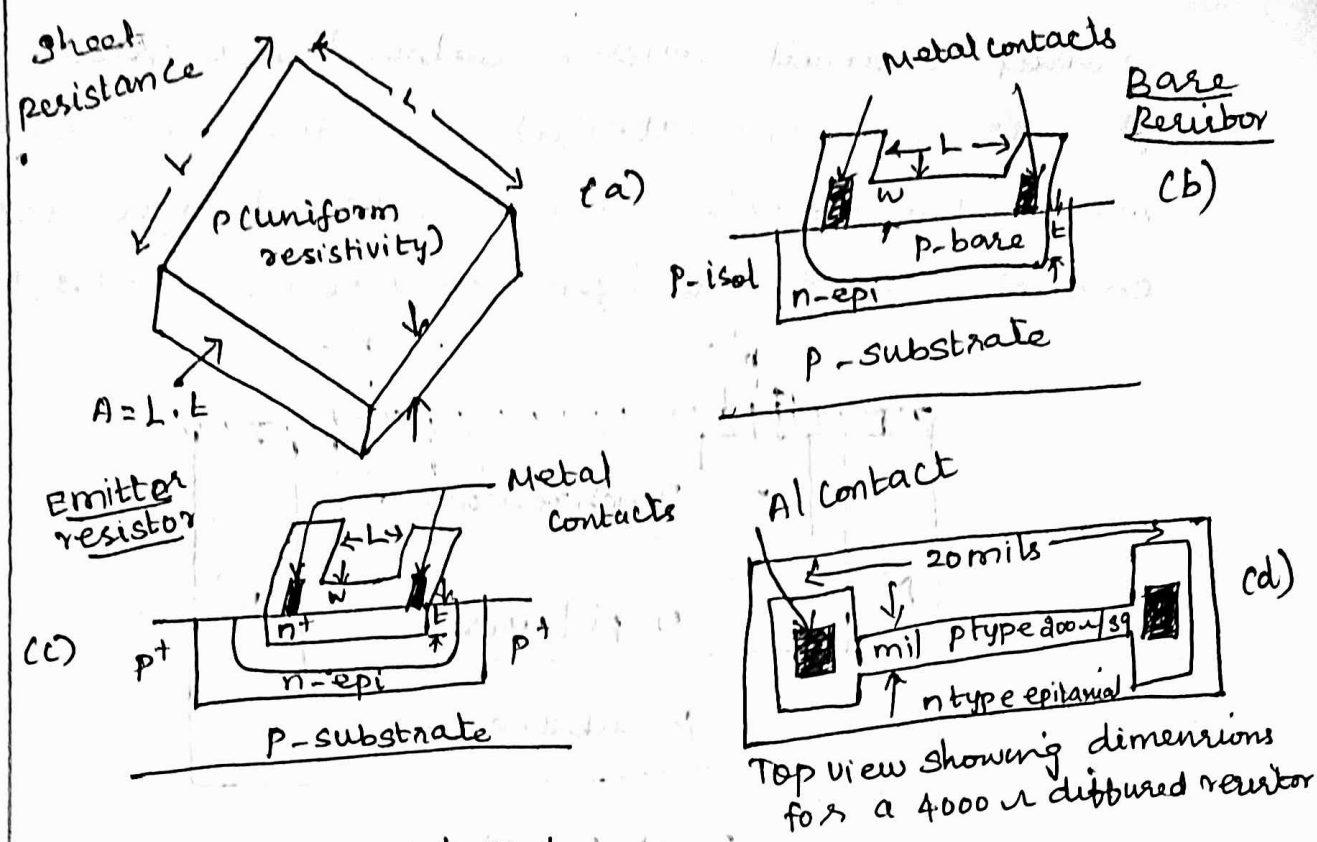
$$R = \rho \times \frac{L}{w \times t} \quad (L, w \rightarrow \text{surface dimensions})$$

$$R = R_S \times \frac{L}{w}.$$

$L/w \rightarrow$ Aspect ratio of the surface geometry.

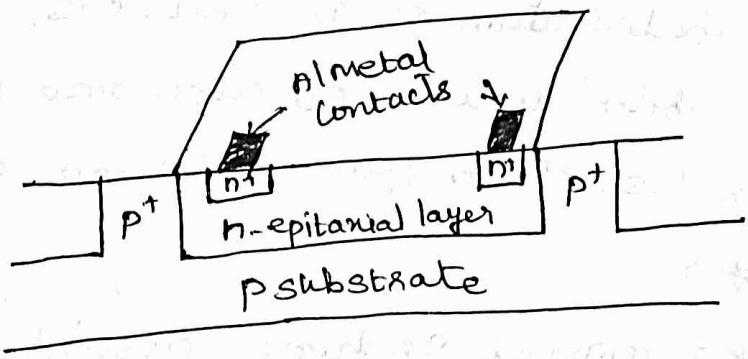
Base resistor : 20 Ω to 300kΩ. (easily fabricated)

Emitter resistor : 10 to 1kΩ, (R_S is 5Ω/sq).



Epitaxial Resistor :-

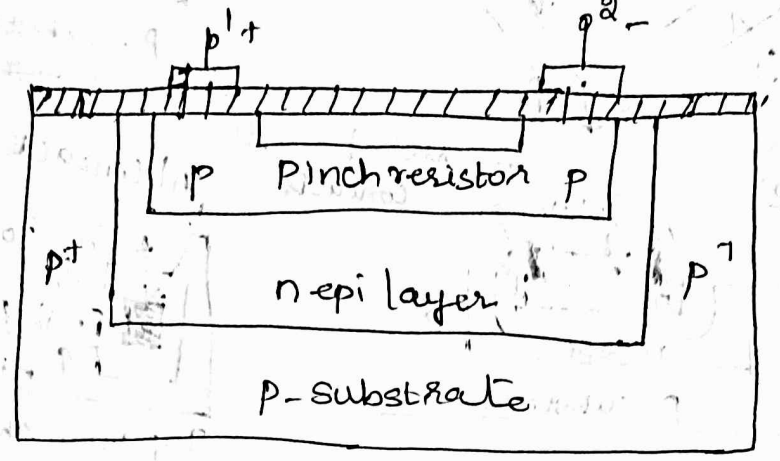
Large value of resistance possible by base or emitter resistor achieved by using n-epitaxial collector region. Rs is 1 to 10 kΩ/sq.



Pinched Resistor :-

The sheet resistivity of a semiconductor region can be increased by reducing its effective cross-sectional area. This technique is used to achieve a high value of sheet resistance from the ordinary base diffused resistor. Resistance : MΩ in small area. In the fig, no current can flow through the n-type material (dark region) due to the diode at contacts in the reverse direction.

⇒ only a small reverse saturation current can flow through n-material. By creating this n-type region, the effective cross sectional area for the conduction path has been reduced, $R = 1/\sigma A$ increases



Pinch Resistor.

Thin Film Resistor :-

Vapour thin film deposition techniques used for the fabrication of Ic resistors. A very thin metallic film usually of nichrome (NiCr) of thickness less than 1μm is vapour deposited on the SiO_2 layer.

Using masked etching, desired geometry of this film is achieved to obtain suitable values of resistors. Ohmic contacts are made using Al metallization.

Nichrome resistors are available with R_S of 40 to 400Ω/square, Resistance 20 to 50kΩ Obtained.

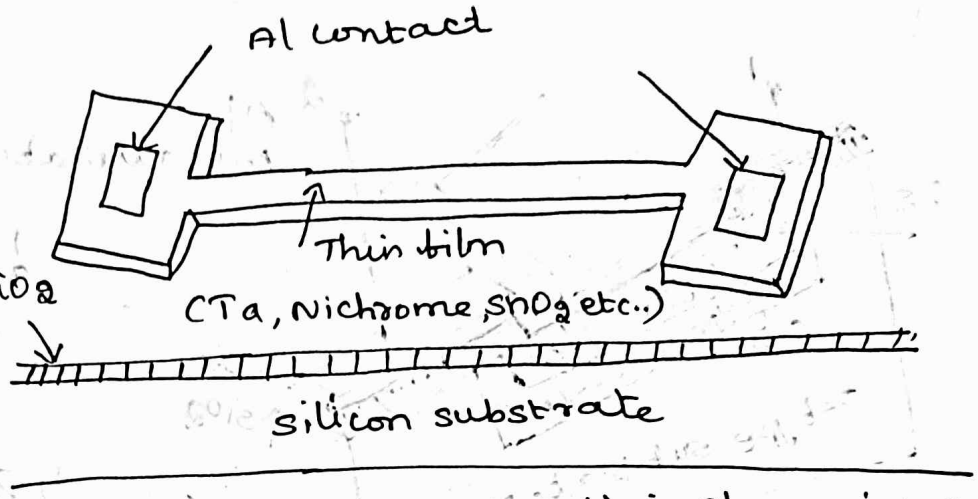
Advantages :-

1) It has lesser and smaller parasitic components and high frequency behaviour is better.

2) The values of thin-film resistors easily adjusted after fabrication by cutting a part of the resistor with a laser beam.

3) Low temp co-efficient, more stable.

Higher value of resistor obtained by depositing Tantalum over SiO_2 layer. Disadvantages is additional process steps required for fabrication.



Cross section of a thin film resistor.

Fabrication of capacitance

Two commonly used methods are

1) Junction capacitor

2) MOS and thin film capacitor.

1) Junction capacitor :-

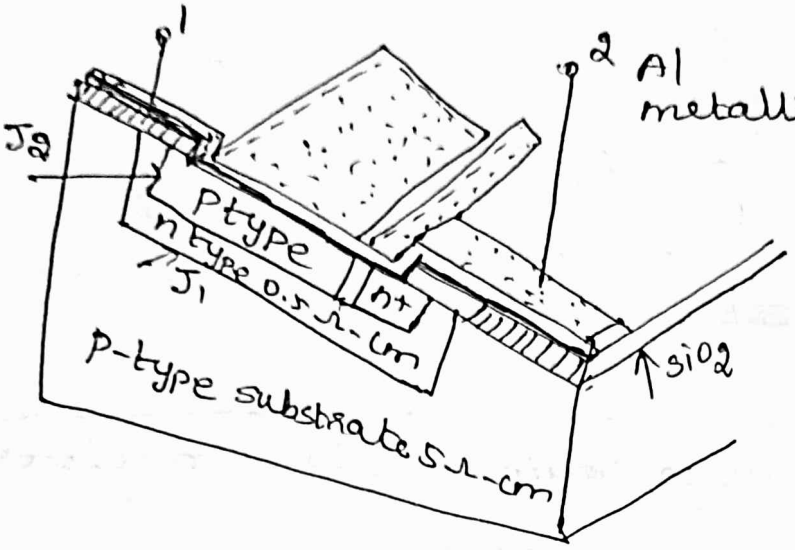
There are two junctions in this type of diffused capacitor. Junction J_2, if reverse bi produce the desired capacitance. A parasitic capacitance C_1 is inevitable due to the junct between n-type epitaxial layer and the substra

In the equivalent circuit, two diodes are the idealized diodes of the two junctions.

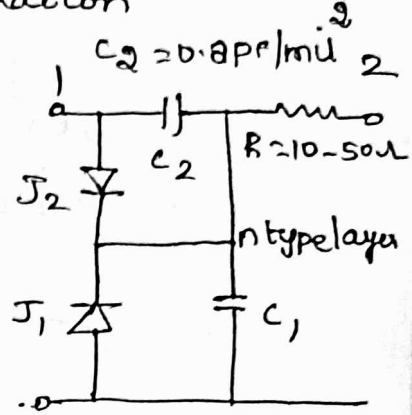
⇒ The substrate held at most negative point to minimize C_1.

⇒ The value of the C_2 depend upon the area of the junction, impurity concentration of the n-type epitaxial layer, voltage across the junction.

⇒ C_2 is polarised, and obtained when J_2 is R.B.



Junction type IC capacitor



Equivalent circuit

MOS and Thin film capacitor :-

⇒ It is barically a parallel plate capacitor with SiO_2 as the dielectric.

⇒ The heavily doped n+ region formed during emitter diffusion forms the lower plate.

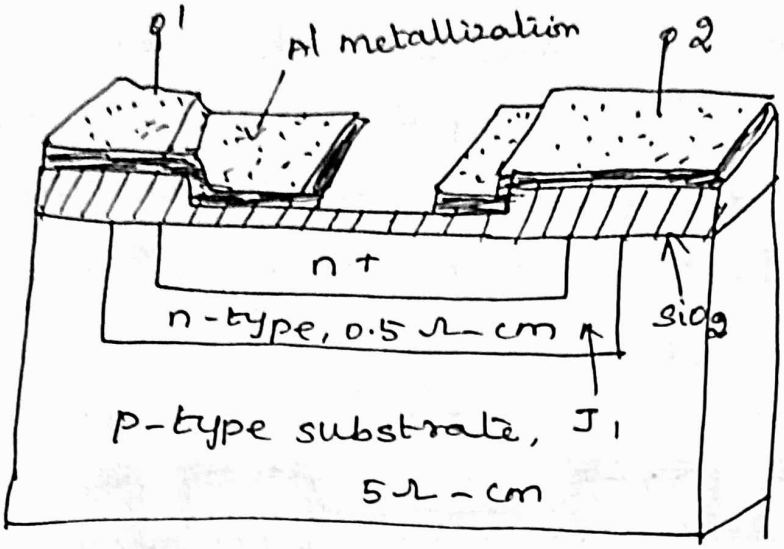
⇒ Thin film of aluminium metallization forms the upper plate of the capacitor with SiO_2 as the dielectric

Advantage : Nonpolar.

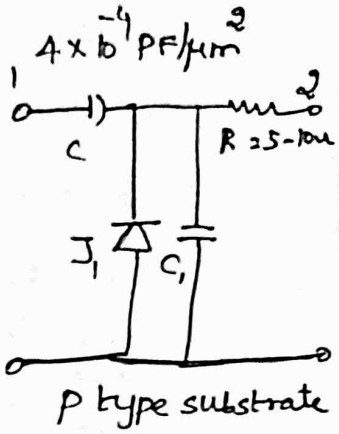
Silicon Nitride (Si_3N_4) used as a dielectric layer.

⇒ It requires a number of additional masking and deposition steps.

⇒ Aluminium or tantalum used as capacitor plates and aluminium oxide (Al_2O_3) or tantalum oxide (Ta_2O_5) as dielectric material.



Structure



Equivalent circuit of a MOS capacitor.

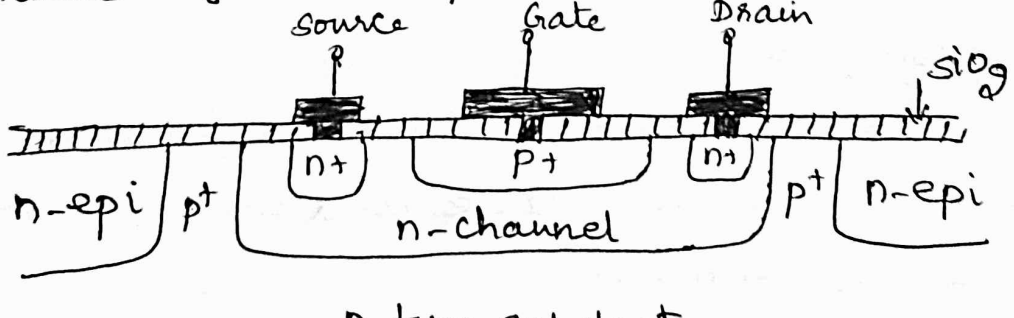
Fabrication of FET :-

JFET Fabrication :-

⇒ The epitaxial layer which formed the collector of the BJT is used as the n-channel of the JFET.

⇒ The p+ gate is formed in the n-channel by the process of diffusion or ion-implantation.

⇒ The n+ regions formed under the drain and source contact regions to provide good ohmic contact.



n-channel JFET structure.

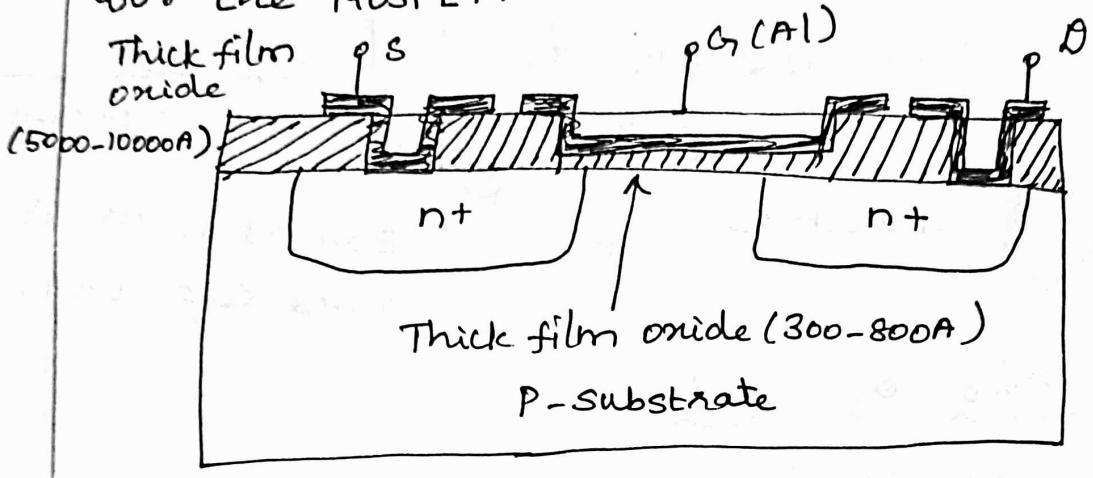
MOSFET Fabrication :-

i) Enhancement type

ii) Depletion type

N-Channel Enhancement MOSFET :-

The metallic gate G is separated from the semiconductor channel by the insulating SiO_2 layer. The insulating layer of silicon dioxide gives an extremely high input resistance (10^{10} to $10^{15}\Omega$) for the MOSFET.



n-channel MOSFET.

V_T → 3 to 6V ; power supply voltage : 12 V → drain supply

Use of Silicon Nitride (Si_3N_4)

Si_3N_4 sandwiched between two SiO_2 layers and provides necessary barrier to prevent impurities penetrating through SiO_2 layer.

Polysilicon Gate :-

Polycrystalline silicon doped with phosphorus is conductive and used gate electrode instead of aluminium.

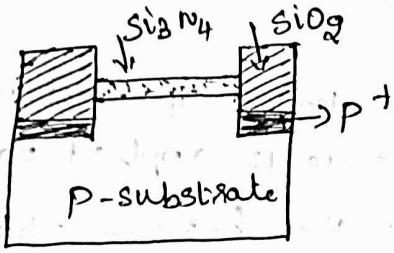
=> Si_3N_4 is coated on the entire surface of a p-type wafer.

=> With help of mask, source, gate and drain included.

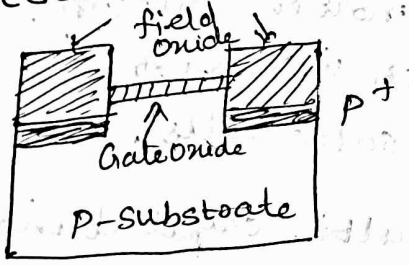
=> Si_3N_4 is etched away from the outside of transistor region.

=> p+ impurities are ion-implanted in the exposed p-substrate.

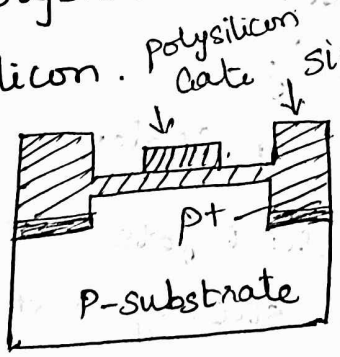
=> A thick SiO_2 layer called field oxide is grown over the p+ regions.



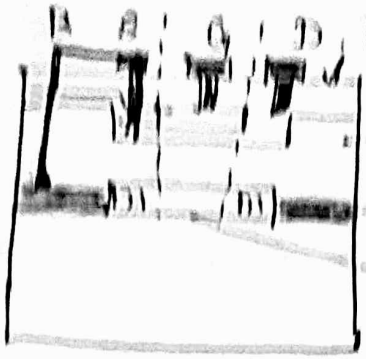
Si_3N_4 is removed by selective etching and SiO_2 layer (800 to 1000A°) is grown over the transistor area.



Polysilicon is now deposited over the entire wafer. The polysilicon gate is formed by selective removal of polysilicon.



The n+ source and drain regions are formed by ion implantation. The field oxide and the polysilicon gate prevent the penetration of dopants below these regions. Drain and source regions are formed.



PV cell fabrication process :

⇒ Before making a silicon wafer, pure silicon is needed which needs to be recovered by reduction and purification of the impure silicon dioxide in quartz.

⇒ Crushed quartz is put in a special furnace and then a carbon electrode is applied to generate a high temperature electric arc between the electrode and the silicon dioxide. It reduces the oxygen from the silicon dioxide and produces carbon dioxide at the electrode and molten silicon. This molten silicon is 99% pure which is insufficient to be used for processing into a solar cells.

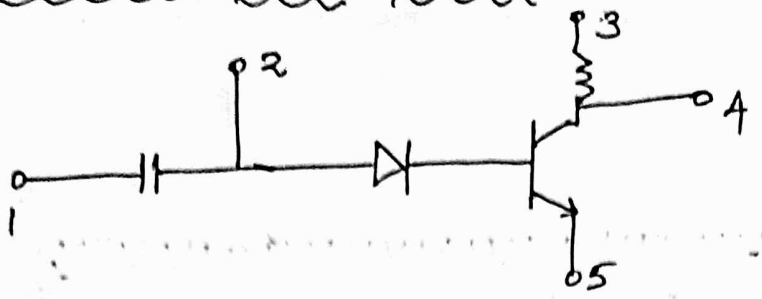
In order to make multi-crystalline silicon cells various methods exist :

1) Heat exchange method.
2) Electro magneto casting
3) Directional solidification system.

⇒ During the casting of the ingots, silicon is often already pre-doped before slicing and selling the wafer disks to the manufacturers.

⇒ These p type and n type doping materials are mostly boron which has 3 electrons (3 valent) and phosphorous (5 electrons) used for n type doping

Fabrication of a Typical circuit :-



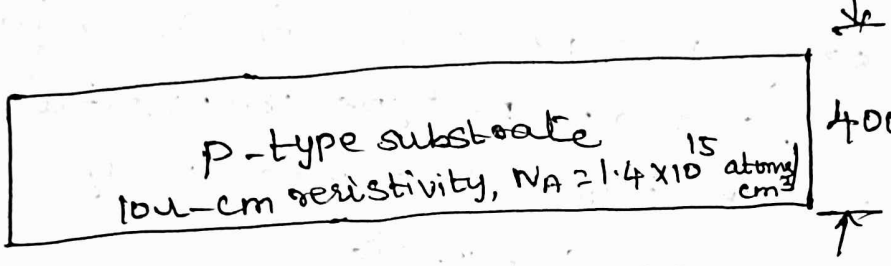
Step1 Wafer Preparation :-

The starting material called the substrate is a p-type silicon waber prepared.

Waber diameter : 10 cm, 0.4 mm (400 μm) thickness.

Resistivity : 10Ω-cm,

Concentration of acceptor atom, $N_A = 1.4 \times 10^{15}$ atoms/cm^3.

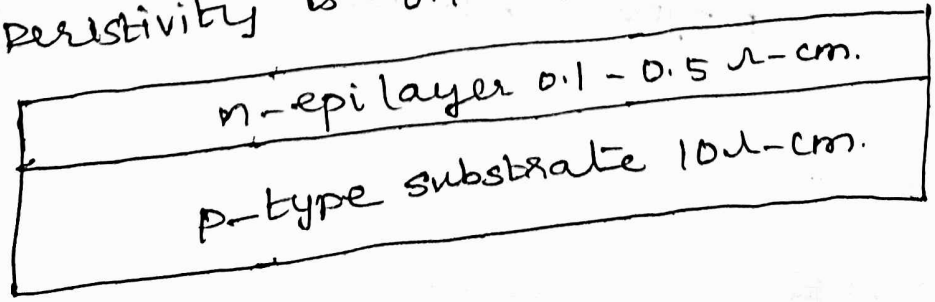


Step2 : Epitaxial Growth :

⇒ An n-type epitaxial film (5-25μm) is grown on the p-type substrate. It becomes collector region of the transistor, element of the diode, diffused capacitor.

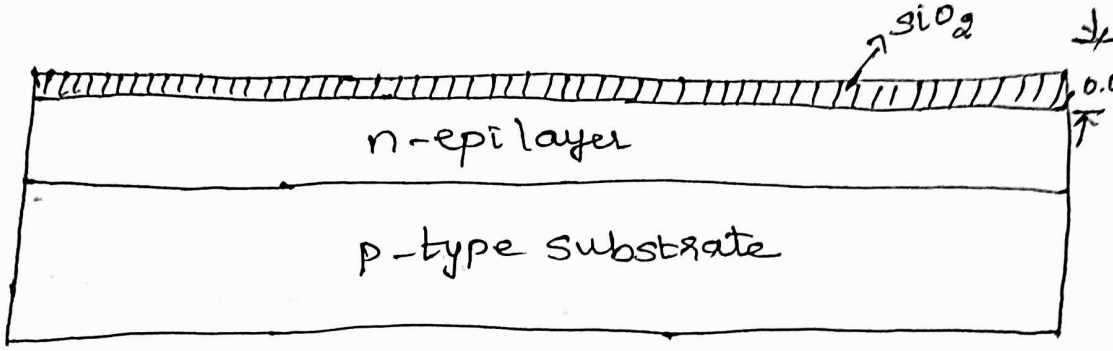
⇒ All active & passive components are fabricated.

⇒ Resistivity is 0.1 to 0.5 Ω cm.



Step 3 : Oxidation

A SiO_2 layer of thickness of the order of 0.02 to 2 μm is grown on the n-epitaxial layer.

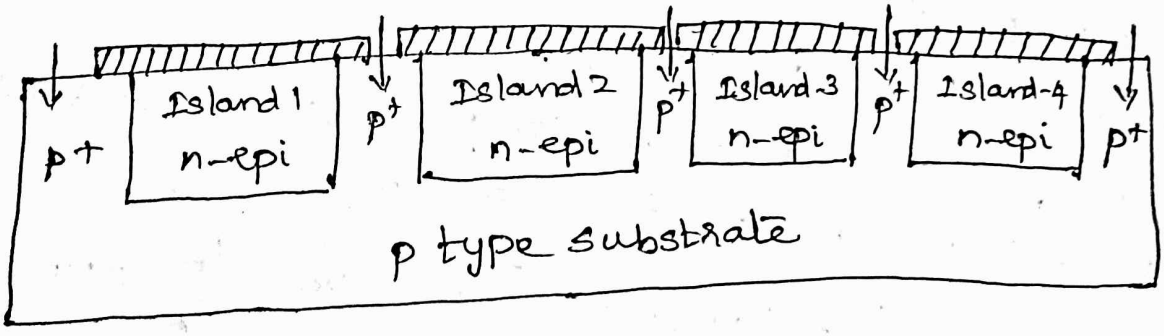


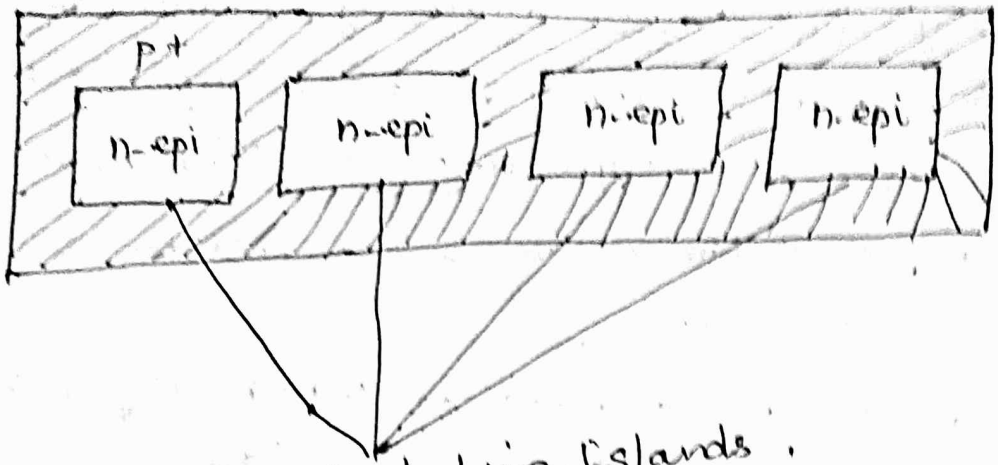
Step 4 : Isolation Diffusion :-

In the given circuit, four components have to be fabricated. So, four islands are required and isolated. So, SiO_2 is removed from five different places using photolithographic technique

⇒ Then heavy p-type diffusion for a long time interval, so that p-type impurities penetrate the n-type epitaxial layer and reach the p-type substrate.

⇒ The concentration of $N_A = 5 \times 10^{20}\ cm^{-3}$ in the region between isolation islands is kept higher than p-type substrate ($N_A = 1.4 \times 10^{15}$ atoms/cm^3)

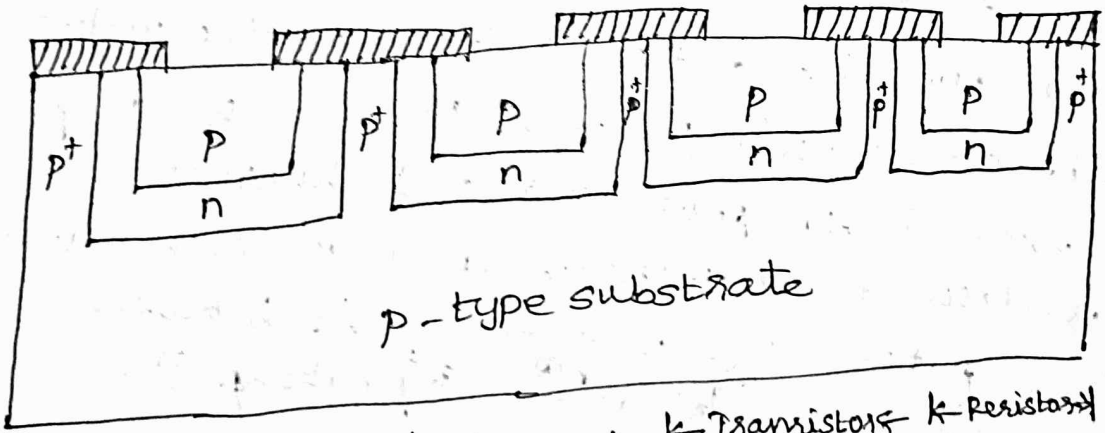




Step(5) Base Diffusion :-

=> A new layer of SiO_2 is grown over the entire wafer and a new pattern of openings is formed using photolithographic Technique.

=> P-type impurities such as boron are diffused through the openings. It does not penetrate through n-layer into the substrate. This diffusion is used to form base region of the transistor, resistor, anode of the diode, Junction capacitors.



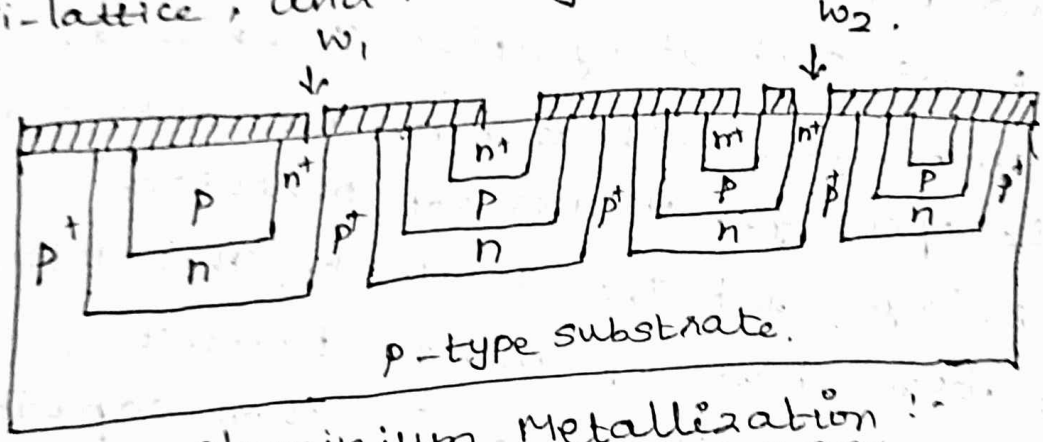
← capacitor → ← Diode → ← Transistor ← Resistor →

Step 6 Emitter Diffusion :-

=> A new layer of SiO_2 is again grown over the entire wafer and selectively etched to open a new set of windows & n-type impurity (phosphorous) is diffused. This forms transistor emitter & cathode region of diode.

=> windows (W_1, W_2 etc) also etched into n-region where contact is to be made to the n-type layer.

=> Heavy concentration of phosphorous ($2 \times 10^{20} cm^{-3}$) doping causes a high degree of damage to the Si-lattice, and making it semi-metallic.

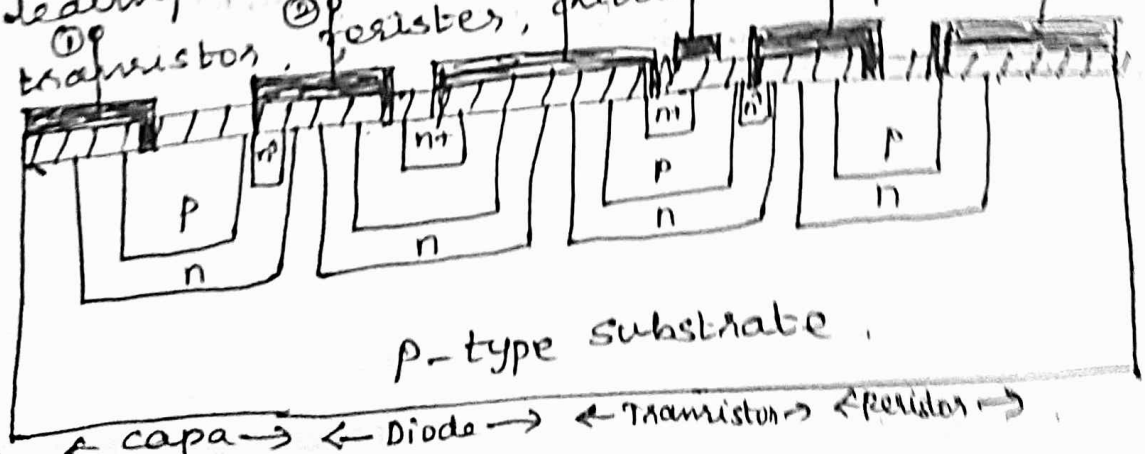


Step 7 Aluminium Metallization :-

=> A thin even coating of aluminium is vacuum deposited over the entire surface of the wafer.

=> The interconnection pattern between the components is then formed by photo-resist techniques.

=> The undesired aluminium areas are etched away leaving a pattern of interconnections between transistor ①, resistor ②, diode ③ & capacitor ④.



UNIT-II Dc characteristics

⇒ An ideal op-amp draws no current from the source

⇒ In real op-amp, current is taken from the source into the op-amp inputs.

⇒ Real op-amp dependent of temperature

D.C characteristics are

1) Input bias current
2) Input offset current
3) Input offset voltage
4) Thermal drift.

1) Input Bias current :-

→ The op-amp's input is a dibberential amplifier, made of BJT or FET.

→ To supply current into the bases by the external circuit, the transistor must be biased.

→ In practical op-amp a small value of dc current is passed to the input terminals to bias the input transistors.

→ The base current entering into the inverting & non-inverting terminals

are I_B^- and I_B^+.

$\Rightarrow$ I_B^- & I_B^+ are not exactly equal due to internal imbalances between the two inputs.

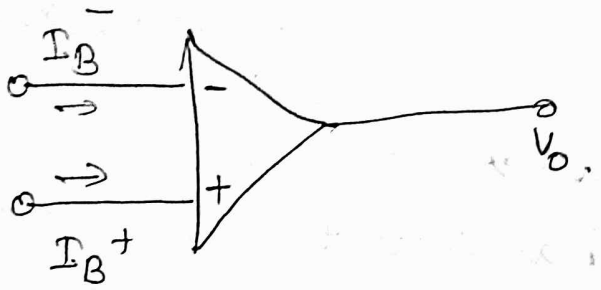


fig: 1 Input Bias current.

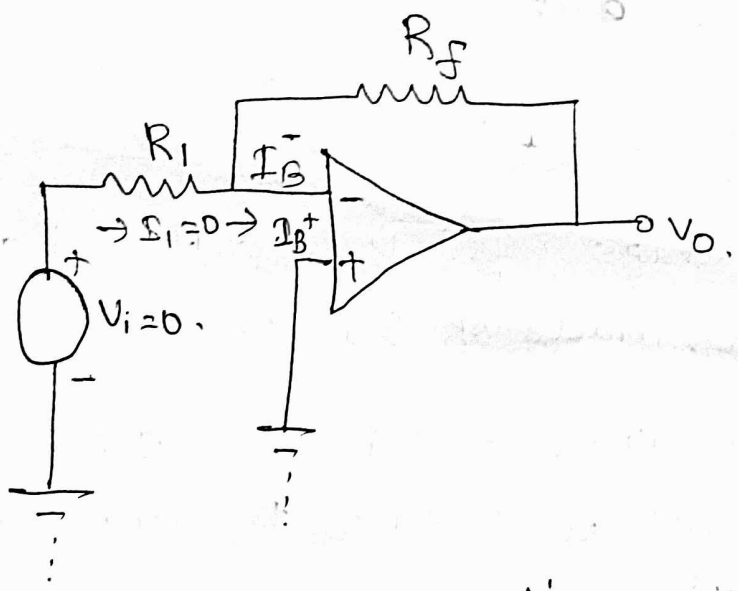


fig: 2. Inverting amplifier with bias currents.

$$I_B = \frac{I_B^+ + I_B^-}{2}$$

For 741, a bi-polar op-amp the bias current is 500nA or less.

For FET input op-amp bias currents as low as 50pA.

If input voltage V_i is set to zero volt,

$V_o = 0V$.

$$V_o = (I_B^-) R_f .$$

for 741 op-amp, 1MΩ feedback Resistor,

$$V_o = 500nA \times 1M\Omega .$$

$$= 500mV .$$

The output is driven to 500mV, with zero input due to bias currents.

⇒ This effect can be compensated by using a compensation Resistor Rcomp added between the non inverting input terminal and ground.

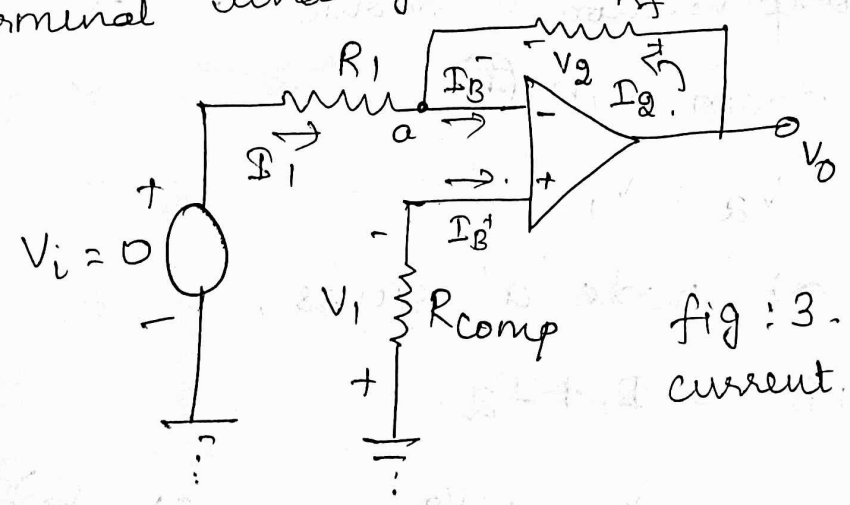


fig: 3. Bias current compensation

current I_B^+ flowing through Rcomp develops a voltage V_1 across it.

using KVL,

$$-V_i + 0 + V_2 - V_o = 0 .$$

$$V_o = V_2 - V_1. \quad \text{—(I)}$$

By proper value of R_{comp},

V_2 cancelled with V_1.

So, $V_o = 0$.

$$V_1 = I_B^+ R_{comp}.$$

$$I_B^+ = \frac{V_1}{R_{comp}}.$$

The voltage at node a, is $-V_1$.

$$I_1 = \frac{V_1}{R_1}.$$

$$I_2 = \frac{V_2}{R_f}.$$

For compensation V_o should be zero,

So from eqn (I),

$$V_2 = V_1.$$

KCL at node 'a' gives,

$$I_B^- = I_1 + I_2.$$

$$= \frac{V_1}{R_1} + \frac{V_2}{R_f} \qquad (V_1 = V_2).$$

$$= \frac{V_1}{R_f} + \frac{V_1}{R_1}.$$

$$I_B^- = V_1 \left(\frac{R_1 + R_f}{R_1 R_f} \right) \quad \text{---(II)}$$

Assume $I_B^- = I_B^+$,

$$I_B^+ = \frac{V_1}{R_{comp}}$$

By using above 2 equations & Sub eqn (II),

$$\frac{V_1}{R_{comp}} = \frac{V_1 (R_1 + R_f)}{R_1 R_f}$$

$$R_{comp} = \frac{R_1 R_f}{R_1 + R_f} = R_1 \| R_f$$

To compensate for bias currents, the compensating resistor R_{comp} should be equal to the parallel combination of resistors tied to the inverting terminal.

Input offset current :-

⇒ Bias current compensation will work if both I_B^+ & I_B^- are equal.

⇒ But in practical, always small difference between I_B^+ & I_B^-. This difference is called the offset current (I_{os}).

$$|I_{os}| = I_B^+ - I_B^-$$

I_{os} for BJT Op-amp is 200nA.

I_{os} for FET Op-amp is 10pA.

From fig ③,

$$V_1 = I_B^+ R_{comp}.$$

$$I_1 = \frac{V_1}{R_1}.$$

KCL at node 'a' gives,

$$I_2 = (I_B^- - I_1)$$

$$= I_B^- - \frac{V_1}{R_1}$$

$$I_1 = \frac{V_1}{R_1}.$$

$$V_1 = I_B^+ R_{comp}.$$

$$\boxed{I_1 = \frac{I_B^+ R_{comp}}{R_1}}.$$

$$I_Q = I_B^- - \left(I_B^+ \frac{R_{comp}}{R_1} \right).$$

$$V_0 = I_Q R_f - V_1.$$

$$= I_Q R_f - I_B^+ R_{comp}.$$

$$= \left(I_B^- - I_B^+ \frac{R_{comp}}{R_1} \right) R_f - I_B^+ R_{comp}.$$

$$R_{comp} = \frac{R_1 R_f}{R_1 + R_f}.$$

$$V_0 = \frac{I_B^- R_1 R_f - I_B^+ R_{comp} R_f}{R_1} - I_B^+ R_{comp}.$$

$$= \frac{I_B^- R_1 R_f - I_B^+ R_{comp} R_f - I_B^+ R_{comp} R_1}{R_1}$$

$$= \frac{R_f \left[I_B^- R_1 - I_B^+ R_{comp} \right] - I_B^+ R_{comp} R_1}{R_1}$$

$$V_0 = R_f \left[I_B^- - I_B^+ \right].$$

$$\boxed{V_0 = R_f I_{OS}}.$$

The effect of offset current can be minimized by keeping feedback resistance small.

=) The effect of offset current can be minimized by keeping feedback resistance small.

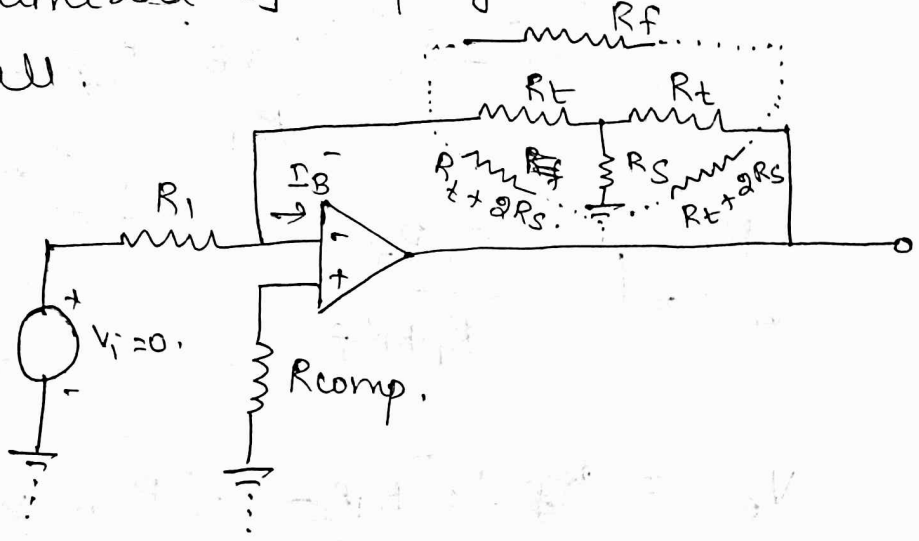


Fig shows T- feedback network.

The T-network provides a feedback signal as if the network were a single feedback resistor.

$$R_t << \frac{R_f}{2}.$$

$$R_S = \frac{R_t^2}{R_f - 2R_t}$$

Input offset voltage :-

=) whenever both the input terminals of the op-amp are grounded, the output voltage should be zero.

=) But in practical, op-amp shows a small non zero output voltage.

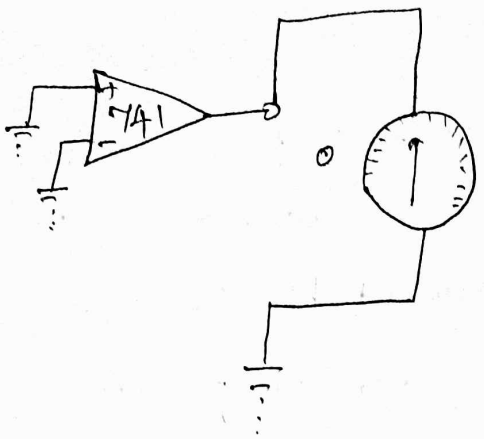
=) To make this output voltage zero, a small voltage in millivolts is required to be applied to one of the input terminals such a voltage makes the output exactly zero.

=) This d.c voltage which makes the output voltage zero, when the other terminal is grounded is called input offset voltage. denoted by V_{ios}.

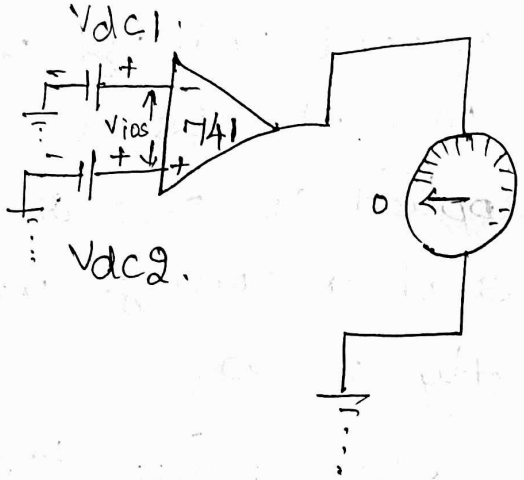
=) The Vios can be +ve (or) -ve. Mentioned in the data sheet.

=) Smaller the value of Vios better is the matching of the input terminals.

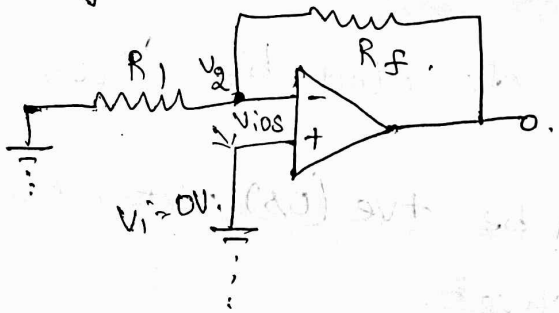
=) Vios depends on the temperature.



$V_{ios} = |V_{dc1} - V_{dc2}|$.



For op-amp 741 C, the input offset voltage is 6mV.



$$V_2 = \left(\frac{R_1}{R_1+R_f}\right) V_o .$$

$$V_o = \left(\frac{R_1+R_f}{R_1}\right) V_2 = \left(1 + \frac{R_f}{R_1}\right) V_2 .$$

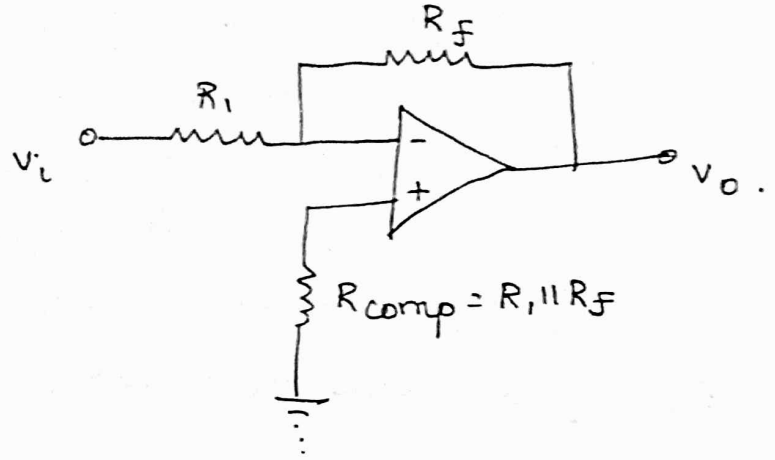
$V_{ios} = |V_i - V_2|$, $V_i = 0$.

$V_{ios} = |0 - V_2| = V_2$.

$$\boxed{V_o = \left[1 + \frac{R_f}{R_1}\right] V_{ios}}$$

Basic op-amp Applications :-

① Scale changer / Inverter :-



⇒ If the ratio $\frac{R_f}{R_1} = k$

where k → real constant.

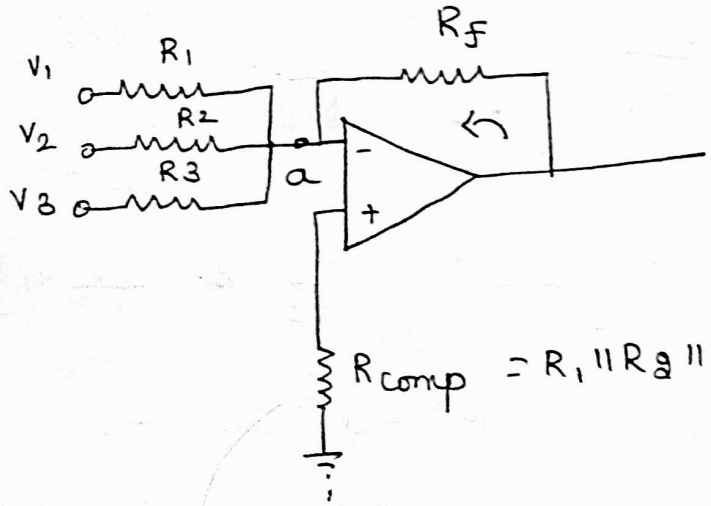
Closed loop gain $A_{CL} = -k$.

$R_f = R_1$, $A_{CL} = -1$.

The circuit is called an Inverter.

The output is 180° out of phase with respect to input.

② Summing Amplifier :-



=) op-amp may be used to design a circuit whose output is the sum of several input signals. such a circuit is called a summing Amplifier or a summer.

Inverting summing Amplifier :-

=) A typical summing amplifier with three input voltages V_1, V_2, V_3 & three input resistors R_1, R_2, R_3 & Feedback Resistor R_f is shown in fig.

=) For an ideal op-amp,

$A_{OL} = \infty$, $R_i = \infty$.

Input bias current is assumed to be zero.

The voltage at node a is zero, non-inverting input terminal is grounded.

KCL at node 'a',

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_o}{R_f} = 0.$$

$$-\frac{V_o}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}.$$

$$V_o = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right].$$

The output is an inverted, sum of the inputs.

In the special case,

$R_1 = R_2 = R_3 = R_f$, $V_o = -[V_1 + V_2 + V_3]$.

when, $R_1 = R_2 = R_3 = 3R_f$.

$$V_o = -\left[\frac{V_1 + V_2 + V_3}{3}\right].$$

Output is the average of the input signals. (Inverted).

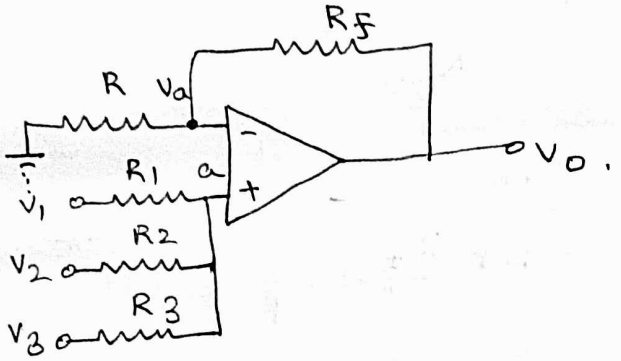
To find R_{comp},

make all inputs $V_1 = V_2 = V_3 = 0$.

Effective input resistance $R_i = R_1 \| R_2 \| R_3$.

$$R_{comp} = R_i \| R_f.$$

Non-inverting summing Amplifier :-



⇒ The voltage at the (-) input terminal be V_a, voltage at (+) input terminal also V_a.

The nodal equation at node a is given by,

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0.$$

$$V_a = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

$$\frac{V_1}{R_1} - \frac{V_a}{R_1} + \frac{V_2}{R_2} - \frac{V_a}{R_2} + \frac{V_3}{R_3} - \frac{V_a}{R_3} = 0.$$

$$-V_a\left[\frac{V_1}{R_1} + \frac{1}{R_1} + \frac{V_2}{R_2} + \frac{1}{R_2} + \frac{V_3}{R_3} + \frac{1}{R_3}\right] = 0.$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{V_a}{R_1} + \frac{V_a}{R_2} + \frac{V_a}{R_3}.$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = V_a \left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right].$$

$$V_a = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \quad \text{---(1)}.$$

The op-amp & two resistors R_f, R constitute a non-inverting Amplifier,

$$V_o = \left[1 + \frac{R_f}{R} \right] V_a.$$

$$V_a = \frac{V_o}{1 + \frac{R_f}{R}}. \quad \text{---(2)}.$$

Sub eqn (2) in (1),

$$\frac{V_o}{1 + \frac{R_f}{R}} = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

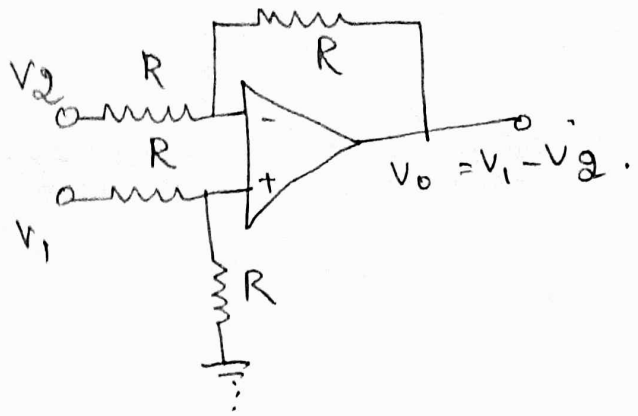
$$V_o = \left[1 + \frac{R_f}{R} \right] \left[\frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \right].$$

which is a non-inverted weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R_f/2$

$V_o = V_1 + V_2 + V_3$.

Subtractor :-



=) If all resistors are equal in value, then the output voltages can be derived using superposition principle.

=) To find output V_{01} due to V_1 alone, make $V_2 = 0$. The above circuit becomes a non-inverting amplifier, input voltage $V_1/2$, at → non-inverting terminal,

$$V_o = \frac{V_1}{2}\left[1 + \frac{R}{R}\right] = V_1.$$

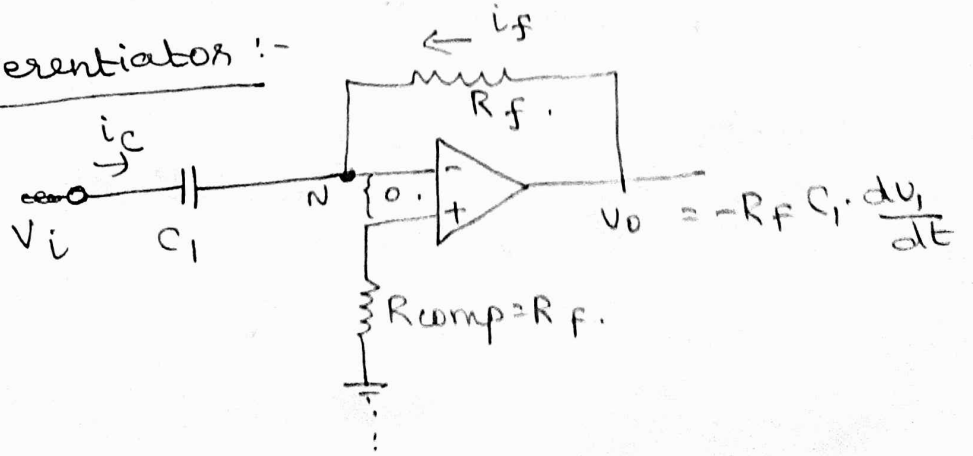
|||ly, the output V_{02}, due to V_2 alone,

$$V_{02} = -V_2.$$

The output voltage V_o due to both the inputs can be written as,

$$V_o = V_{01} + V_{02} = V_1 - V_2.$$

Differentiator :-



The node N is at virtual ground,

$V_N = 0$,

The current i_c through the capacitor is,

$$i_c = C_1 \cdot \frac{d}{dt}[V_i - V_N].$$

$$= C_1 \cdot \frac{dV_i}{dt}.$$

The current i_f through feedback resistor is

$$\frac{V_o}{R_f}.$$

Nodal equation at node N is,

$i_c + i_f = 0$.

$$C_1 \cdot \frac{dV_i}{dt} + \frac{V_o}{R_f} = 0.$$

$$C_1 \cdot \frac{dV_i}{dt} = -\frac{V_o}{R_f}.$$

$$V_o = -R_f C_1 \cdot \frac{dV_i}{dt}.$$

$$\boxed{V_o = -R_f C_1 \cdot \frac{dV_i}{dt}}.$$

Phasor equivalent of above equation is,

$$V_o(s) = -R_f C_1 s V_i(s).$$

V_o, V_i phasor representations of V_o, V_i.

put $s = j\omega$,

$$|A| = \left|\frac{V_o}{V_i}\right| = \left|-j\omega R_f C_1\right|.$$

$$= \omega R_f C_1.$$

$$|A| = \frac{f}{f_a}$$

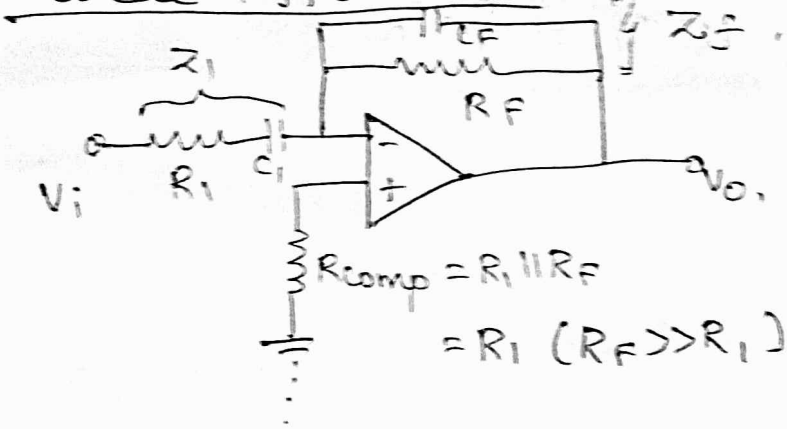
$$f_a = \frac{1}{2\pi R_F C_1}$$

At $f = f_a$, $|A| = 1$ i.e 0 dB.

1) The gain increases at a rate of +20 dB/decade. At high frequency, a differentiator become unstable and break into oscillations.

2) The input impedance $1/\omega C_1$ increases with increase in frequency, circuit is sensitive to high frequency noise.

Practical Differentiator:-



Transfer function is,

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_F}{Z_i} = -\frac{sR_FC_1}{(1+sR_F(F)(1+sC_1R_1)}$$

For $R_F C_F = R_1 C_1$,

$$\frac{V_o(s)}{V_i(s)} = -\frac{sR_FC_1}{(1+sR_1C_1)^2} = -\frac{sR_FC_1}{\left[1+j\frac{f}{f_b}\right]^2}$$

$$f_b = \frac{1}{2\pi R_1 C_1}.$$

f_b should be such that, $\boxed{f_a < f_b < f_c}$.

For good differentiation,

$$T \geq R_F C_1.$$

$$\boxed{V_0 = -R_F C_1 \cdot \frac{dV_i}{dt}}.$$

A good differentiator may be designed by

1) Choose f_s equal to the highest frequency of the input signal. Assume $C_1 \leq 1\mu F$.

2) Choose $f_b = 10 f_a$

calculate R_1 & C_F.

$$R_1 C_1 = R_F C_F.$$

Ideal op-amp Characteristics :-

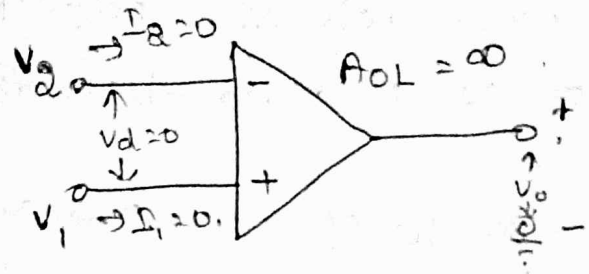


Fig shows an ideal op-amp. It has 2 input signals V_1, V_2 applied to non-inverting and Inverting terminals.

1) An ideal op-amp draws no current at both the input terminals. i.e $I_1 = I_2 = 0$. Input impedance is infinite.

2) The gain of an ideal op-amp is infinite (∞). hence the differential input $V_d = V_1 - V_2$ is zero for the finite output voltage V_o.

1) Infinite voltage gain :-

$A_{OL} = \infty$.

It is the differential open loop gain and is infinite for an ideal op-amp.

2) Infinite Input Impedance :-

Input impedance $Z_{in} = \frac{V_{in}}{I_{in}}$

$I_{in} = 0$,

$Z_{in} = \frac{V_{in}}{0} = \infty$

This ensures that no current can flow into an ideal op-amp.

c) Zero output impedance ($R_o = 0$)

The ideal op-amp acts as a perfect internal voltage source with no internal resistance.

Output voltage of the op-amp remains same, irrespective of the value of load resistance connected.

d) Zero offset voltage ($V_{iss} = 0$).

The presence of the small output voltage though $V_1 = V_2 = 0$ is called an offset voltage. It is zero for an ideal op-amp.

e) Infinite bandwidth :-

The range of frequency over which the amplifier performance is satisfactory is called its bandwidth. The bandwidth of an ideal op-amp is infinite.

The gain of the op-amp will be constant over the frequency range from d.c (0 frequency) to ∞ frequency.

f) Infinite CMRR ($\rho = \infty$).

$$CMRR = \frac{\text{Differential gain}}{\text{Common mode gain}}$$

$$CMRR = \left|\frac{A_d}{A_c}\right|.$$

Thus for an ideal op-amp.
common mode gain is 0.
So, CMRR is ∞.

g) Infinite slew rate : (S = ∞).

slew rate defined as the maximum rate of change of output voltage with time expressed in V/μs.

$$\text{slew rate} = S = \left.\frac{dV_o}{dt}\right|_{\text{maximum}}.$$

h) No effect of temperature.

i) Power supply Rejection Ratio :

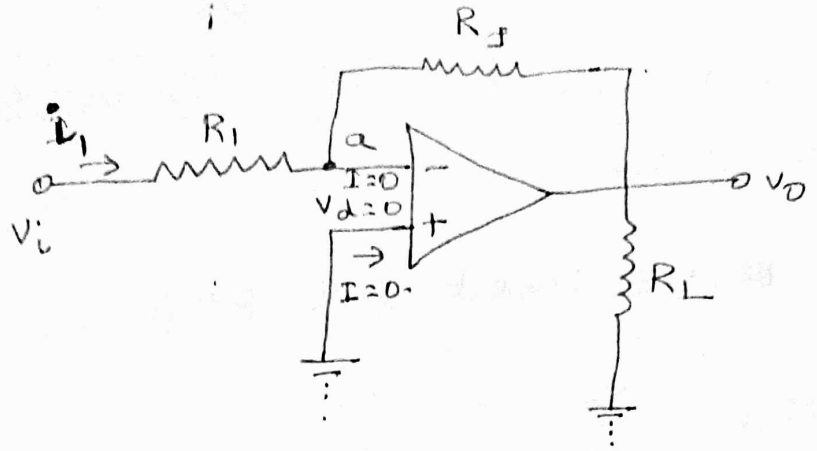
(PSRR = 0)

$$PSRR = \left.\frac{\Delta V_{ios}}{\Delta V_{CC}}\right|_{V_{EE} \text{ constant}}.$$

The power supply rejection ratio is defined as the ratio of the change in input offset voltage due to the change in supply voltage producing it.

Ideal value is zero.

The Inverting Amplifier



⇒ This circuit uses of all the op-amp circuits.

⇒ The output voltage V_o is fed back to the inverting input terminal through the $R_f - R_1$ network.

R_f → Feedback Resistor.

⇒ Input signal V_i applied to the inverting input through R_1, Non-inverting input terminal of op-amp is grounded.

Analysis :-

Assume an ideal op-amp.

node a is at grounded potential.

current i_1 through R_1 is,

$$i_1 = \frac{V_i}{R_1}$$

op-amps draw no current.

output voltage,

$$V_o = -i_1 R_f = -V_i \times \frac{R_f}{R_1}$$

-ve sign indicates a phase shift of 180° between V_i & V_o.

Gain of the inverting amplifier,

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

Nodal Equation at the node 'a' is,

$$\frac{V_a - V_i}{R_1} + \frac{V_a - V_o}{R_f} = 0$$

V_a → voltage at node a. a is at virtual ground. $V_a = 0$,

⇒ The value of R_1 kept large to avoid loading effect.

⇒ Load Resistor R_L is put at the output.

⇒ If Resistances R_1 and R_f are replaced by impedances Z_i & Z_f, then

Voltage gain $\boxed{A_{CL} = -\frac{Z_f}{Z_i}}$ ← (5).

Equation (5) is valid only if the op-amp is an ideal one. For a practical, expression for closed loop voltage gain calculated using low frequency model. fig(b).

Practical Inverting Amplifier:-

The input impedance R_i of an op-amp is usually greater than R_1.

So, assume $V_{eq} = V_i$, $R_{eq} = R_1$.

From the output loop, fig(b),

$$V_o = iR_o + A_{OL}V_d \quad \text{— (1)}$$

$$V_d + iR_f + V_o = 0 \quad \text{— (2)}$$

$$\text{(1)} \Rightarrow \frac{V_o - iR_o}{A_{OL}} = V_d \quad \text{— (3)}$$

Sub (3) in eqn (2),

$$\frac{V_o - iR_o}{A_{OL}} + iR_f + V_o = 0$$

$$V_o - iR_o + iR_f A_{OL} + V_o A_{OL} = 0$$

$$V_o[1 + A_{OL}] - i[R_o - R_f A_{OL}] = 0$$

$$V_o[1 + A_{OL}] = i[R_o - R_f A_{OL}] \quad \text{— (4)}$$

$$i = \frac{V_o(1 + A_{OL})}{(R_o - R_f A_{OL})}$$

KVL loop equation,

$$V_i = i'(R_1 + R_f) + V_o \quad \text{— (5)}$$

put the value i from eqn (4) in eqn (5).

V_i 7.

$$A_{CL} = \frac{V_o}{V_i} = \frac{R_o - A_{OL}R_f}{R_o + R_f + R_1(1+A_{OL})}$$

$A_{OL} >> 1$, $A_{OL}R_1 >> R_o + R_f$.

$$A_{CL} = -\frac{R_f}{R_1}.$$

Input Resistance R_i

$$R_{if} = \frac{V_d}{i}$$

Writing the loop equation and solving for R_{if},

$$V_d + i(R_f + R_o) + A_{OL}V_d = 0.$$

$$\boxed{R_{if} = \frac{R_f + R_o}{1 + A_{OL}}}.$$

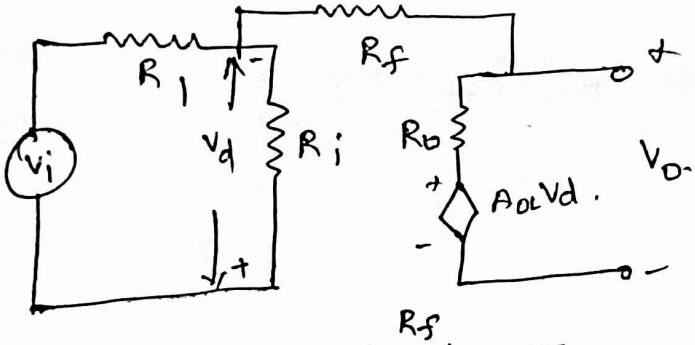


fig (a)

Equivalent circuit of a practical op-amp inverting Amplifier.

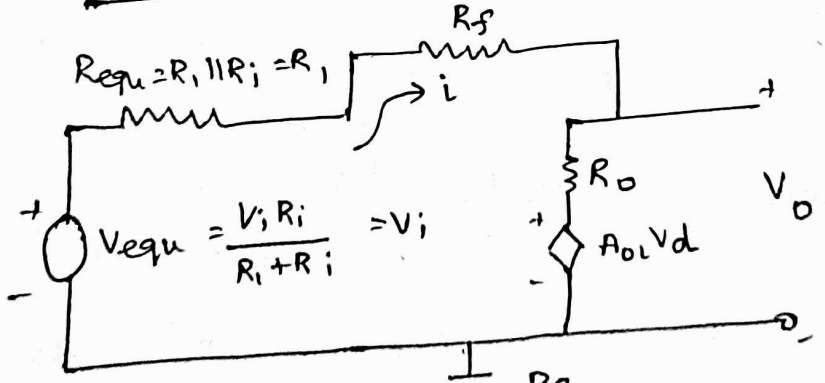


fig (b)

Simplified circuit using Thevenin's equivalent.

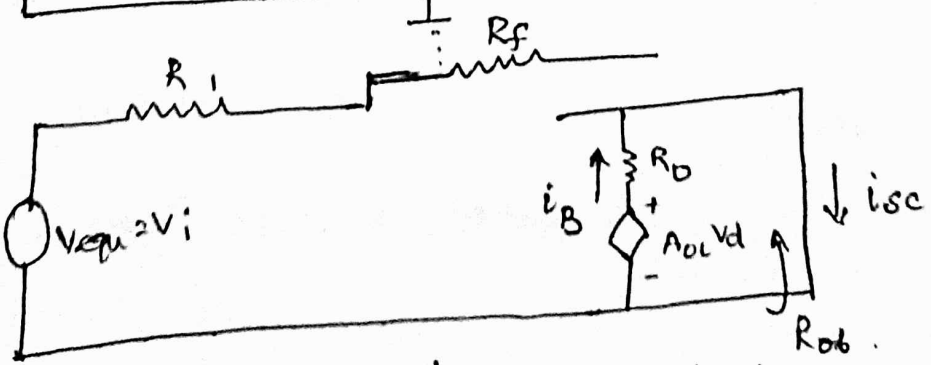


fig (c).

Equivalent circuit for computing R_{ob}.

A.C characteristics.

Frequency Response :

Ideally an op-amp have an infinite bandwidth. If its open loop gain is 90 dB, with d.c signal its gain should remain the same, 90 dB through audio and on to high radio frequencies. The practical op-amp gain, decreases (rolls-off) at higher frequencies.

=) It is because there must be a capacitive component in the equivalent circuit of the op-amp. This capacitance is due to the physical characteristics of the device (BJT or FET) used and internal construction of op-amp.

=) For an op-amp with only one break (corner) Frequency, all the capacitor effects can be represented by a single capacitor C.

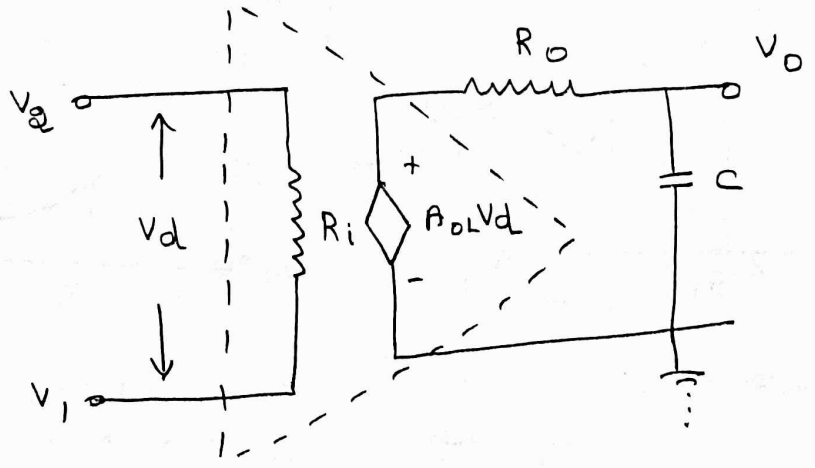


Fig : High Frequency model of an op-amp with single corner Frequency.

The open loop voltage gain of an op-amp is

$$V_o = \frac{-jX_c}{R_o - jX_c} A_{OL} V_d .$$

$$A = \frac{V_o}{V_d} = \frac{A_{OL}}{1 + j 2\pi f R_o C}$$

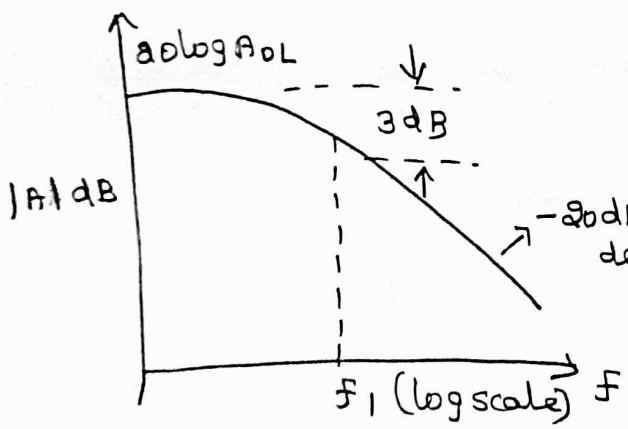
$$A = \frac{A_{OL}}{1 + j(f/f_1)} .$$

$$f_1 = \frac{1}{2\pi R_o C} .$$

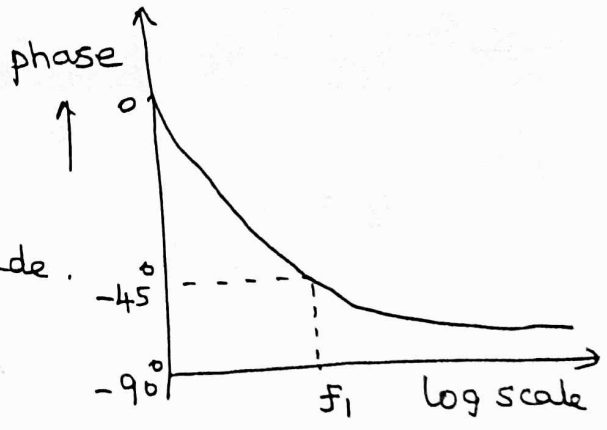
The magnitude and the phase angle of the open loop voltage gain is

$$|A| = \frac{A_{OL}}{\sqrt{1 + (f/f_1)^2}} . \quad \text{— (1)}$$

$$\phi = -\tan^{-1}(f/f_1) . \quad \text{— (2)} .$$



open loop magnitude characteristics in semilog paper



phase characteristics for an op-amp with single break frequency.

=> From the fig, phase characteristics phase angle is zero at frequency $f = 0$. At corner frequency f_1, the phase angle is -45° (lagging), at infinite frequency the phase angle is -90°.

$$A = \frac{A_{OL}}{1 + j(f/f_1)} = \frac{A_{OL}}{1 + j(\omega/\omega_1)}$$

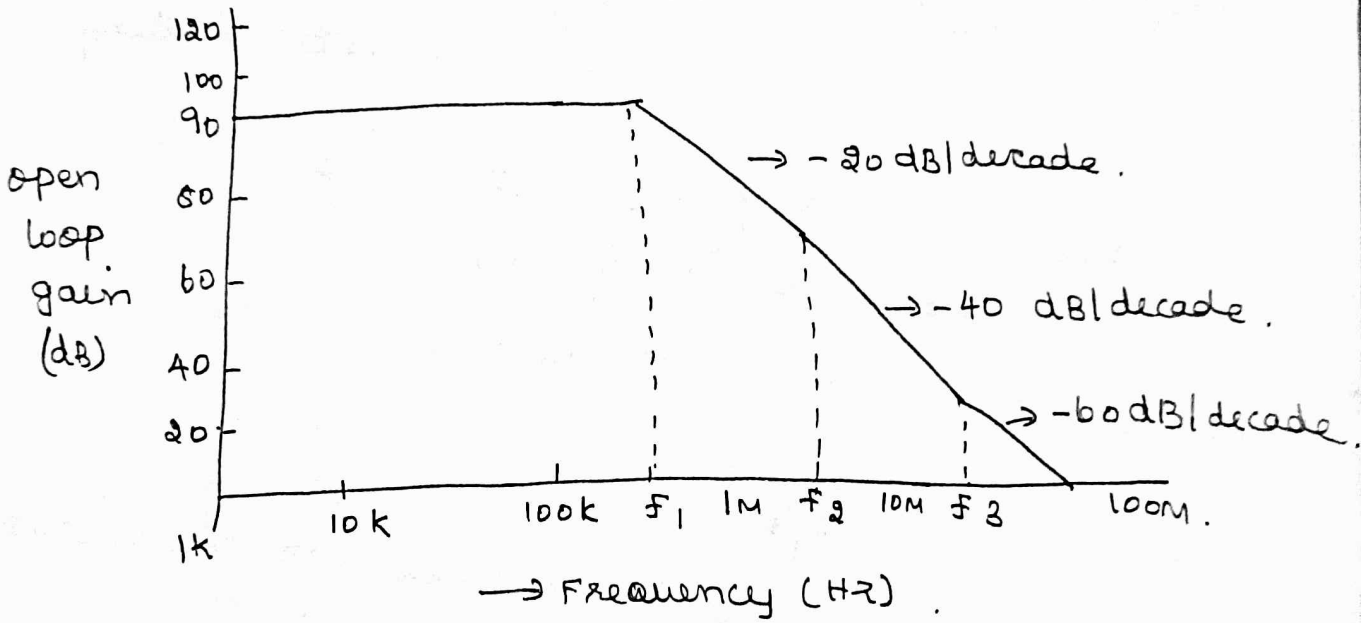
$$= \frac{A_{OL} \cdot \omega_1}{j\omega + \omega_1} \Rightarrow \frac{A_{OL} \cdot \omega_1}{s + \omega_1}$$

The transfer function of an op-amp with three break frequencies can be assumed

$$A = \frac{A_{OL}}{[1 + j f/f_1][1 + j f/f_2][1 + j f/f_3]} \quad 0 < f_1 < f_2 < f_3.$$

$$A = \frac{A_{OL} \cdot \omega_1 \cdot \omega_2 \cdot \omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)}.$$

$0 < \omega_1 < \omega_2 < \omega_3$.



Approximation of open loop gain Vs Frequency curve.

Open loop frequency response is flat (90dB) from low frequencies to 200KHz.

The gain drops from 90 dB to 70 dB, at 200KHz - 2MHz. (-20 dB/decade).

At frequency from 2MHz - 20MHz, rolls off rate is -40 dB/decade.

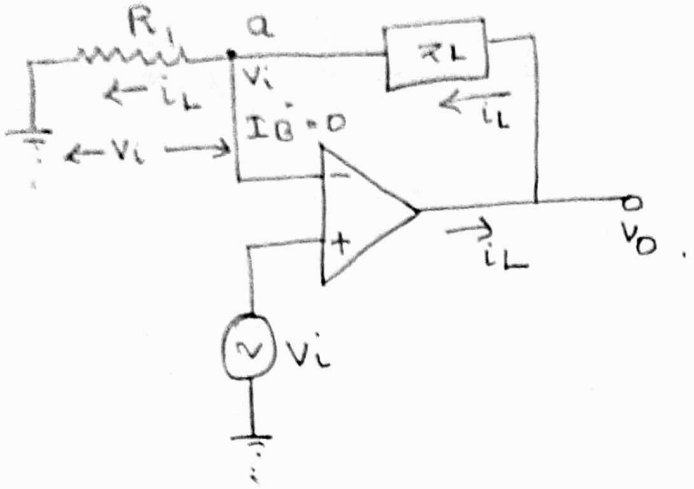
V to I converter :-

Voltage to current converter :-

For many applications, one may have to convert a voltage signal to a proportional output current. For this, two types of circuits possible,

V-I converter with floating load.

V-I converter with grounded load.



Voltage to current converter with floating load.

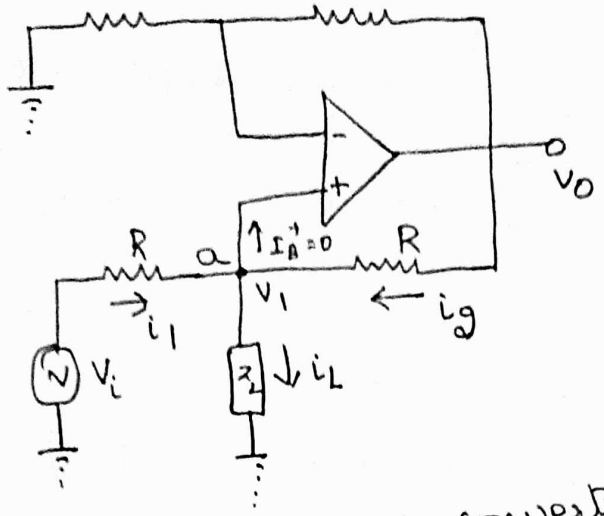
=) In the above ckt ZL is floating.

voltage at node 'a' is Vi,

$$V_i = i_L R_1 \quad (\text{as } I_B = 0).$$

$$i_L = \frac{V_i}{R_1}.$$

The input voltage Vi is converted into an output current of V_i/R_1. The same current flowing through the load and signal source.



Voltage to current converter with grounded load.

Let V_1 be the voltage at node a,

using KVL,

$$i_1 + i_g = i_L$$

$$\frac{V_i - V_1}{R} + \frac{V_o - V_1}{R} = i_L$$

$$V_i + V_o - 2V_1 = i_L R.$$

$$\boxed{V_1 = \frac{V_i + V_o - i_L R}{2}}$$

op-amp is non-inverting mode, the gain of the circuit is $1 + R/R = 2$. The output voltage is,

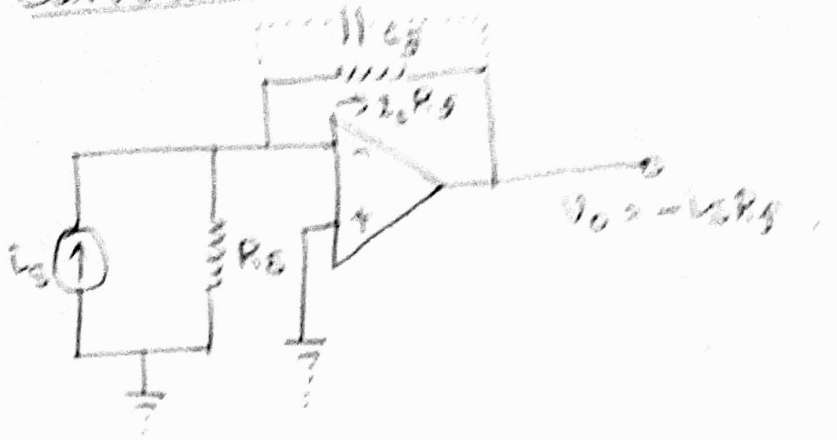
$$V_o = 2 \cdot V_1 = V_i + V_o - i_L R.$$

$$V_i = i_L R.$$

$$i_L = \frac{V_i}{R}.$$

A voltage to current converter is used for low voltage dc and ac voltmeter, LED, zener diode tester.

Current to voltage converter:



=) photocell, photodiode, phototransistor will give an output current that is proportional to an incident radiant energy or light.

=) The current through these devices can be converted to voltage using a I - V converter.

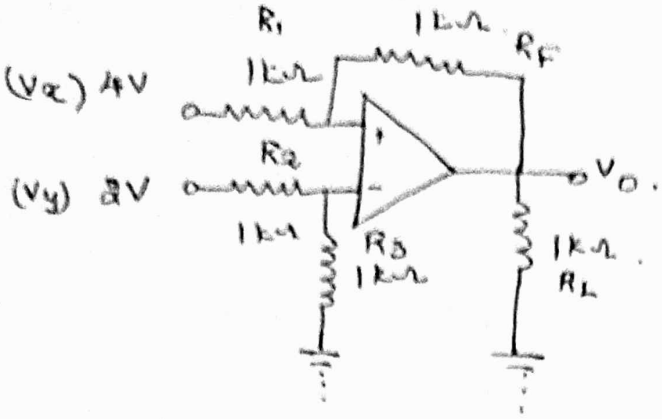
=) (-) input terminal is at virtual ground, no current flows through R_s and current i_s flows through the feedback resistor R_f.

output voltage $V_o = -i_s R_f$.

=) µA741 (I_B = 3nA) used to detect lower currents.

=) Resistor R_f shunted with a capacitor C_f to reduce high frequency noise and possibility of oscillations.

① For the circuit diagram shown below determine the output voltage V_o :-



Solution :-

$R_1 = 1k\Omega$; $V_x = 4V$, $V_y = 2V$.

$R_F = 1k\Omega$.

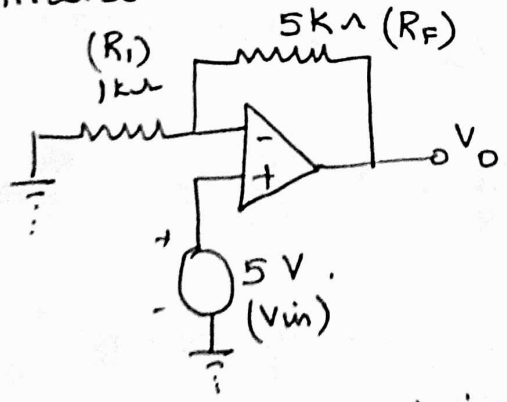
$R_1 = R_2$; $R_F = R_3$.

$$V_O = -\frac{R_F}{R_1}(V_x - V_y).$$

$$= -\frac{1k\Omega}{1k\Omega}(4-2).$$

$$\boxed{V_o = -2V}$$

② Determine the output voltage for the given circuit:



For the non-inverting Amplifier,

$$A_F = 1 + \frac{R_F}{R_1}.$$

$R_1 = 1k\Omega$; $R_F = 5k\Omega$.

$V_{in} = 5V$.

$$\frac{V_o}{V_{in}} = 1 + \frac{R_F}{R_1}.$$

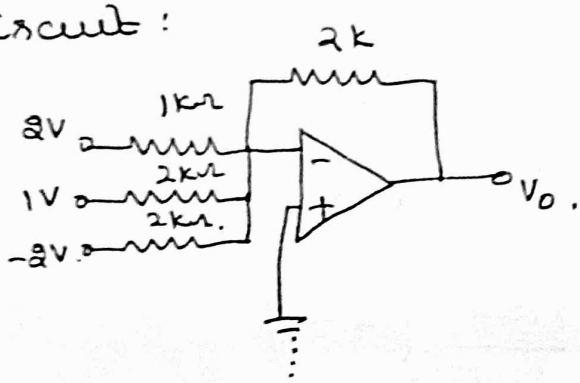
$$= 1 + \frac{5}{1}$$

$$\frac{V_o}{V_{in}} = 6.$$

$$V_o = 6 \times V_{in} = 6 \times 5V = 30V.$$

$$\boxed{V_o = 30V}$$

(ii) Determine the output voltage for the given circuit:



This is an inverting summing Amplifier.

$R_f = 2k\Omega.$

$R_1 = 1k\Omega$; $R_2 = 2k\Omega$, $R_3 = 2k\Omega.$

$V_1 = 2V$, $V_2 = 1V$, $V_3 = -2V.$

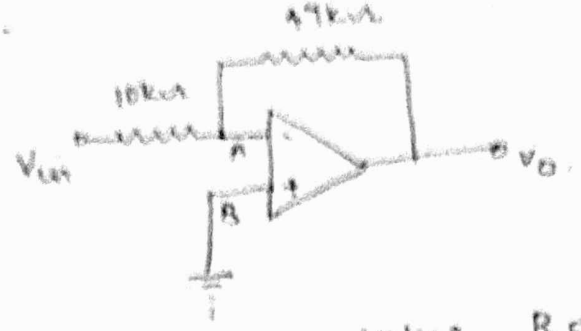
$$V_o = -\left[\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_3} V_3\right].$$

$$= -\left[\frac{2k\Omega}{1k\Omega}(2) + \frac{2}{2}(1) + \frac{2}{2}(-2)\right].$$

$$= -[4 + 1 - 2].$$

$$\boxed{V_o = -3V}$$

① Determine the voltage gain of the op-amp shown in fig :



Given: $R_1 = 10k\Omega$, $R_F = 47k\Omega$.

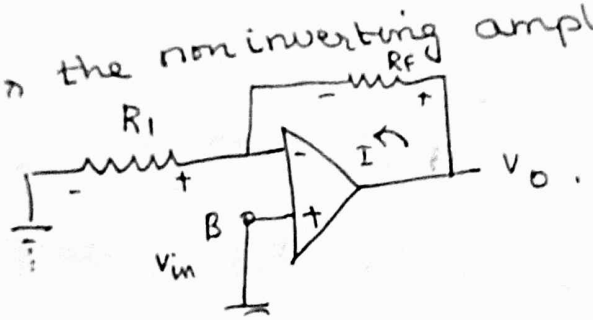
The circuit is inverting Amplifier.

$$\text{Gain} = \frac{V_o}{V_{in}} = -\frac{R_F}{R_1} = \frac{47 \times 10^3}{10 \times 10^3} = -4.7.$$

-ve sign indicates phase shift i.e inverting mode.

② An input of 3V is fed to the non-inverting terminal of an operational Amplifier. The amplifier has $R_i = 10k\Omega$, $R_f = 10k\Omega$, Find the output voltage.

For the non inverting amplifier,



$$A_{VF} = \frac{V_o}{V_{in}} = 1 + \frac{R_F}{R_1}.$$

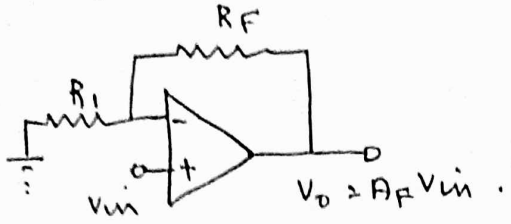
$R_1 = 10k\Omega$, $R_F = 10k\Omega$, $V_{in} = 3V$.

$$A_F = 1 + \frac{10}{10} = 2.$$

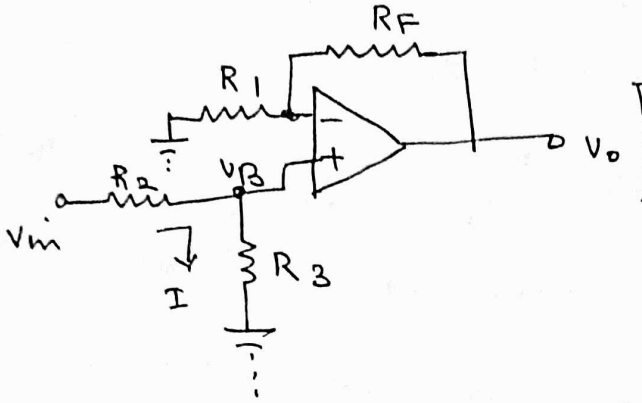
$$A_F = \frac{V_o}{V_{in}} \Rightarrow 2 = \frac{V_o}{3V}.$$

$$\boxed{V_o = 6V}.$$

Key point :- Non inverting Amplifier always amplifies voltage at its non-inverting terminal.



Vin directly applied.



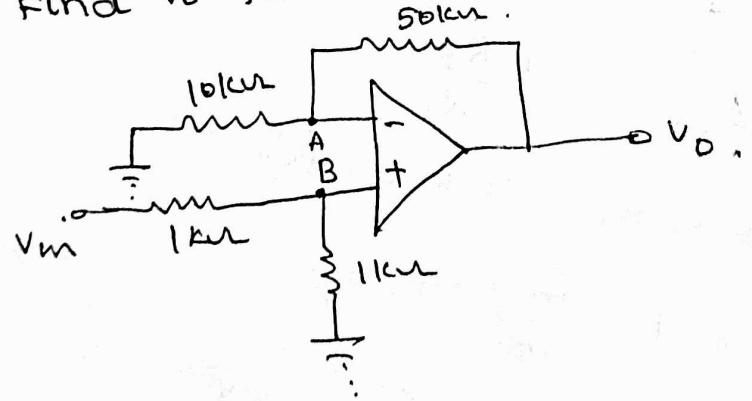
$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_B$$

Vin applied through resistive circuit.

$$V_B = \left[\frac{R_3}{R_2 + R_3}\right] \times V_{in}$$

$$V_o = \left[1 + \frac{R_F}{R_1}\right]\left[\frac{R_3}{R_2 + R_3}\right] \times V_{in}$$

③ Find V_o for the circuit shown below :-



$$V_o = \left[1 + \frac{R_F}{R_1}\right] V_B$$

$$I = \frac{V_{in}}{1\times10^{3} + 1\times10^{3}}$$

$R_2 + R_3 = 1\times10^{3} + 1\times10^{3} = 2\times10^{3}$.

$$V_B = \frac{V_{in} \times R_3}{(R_2 + R_3)}$$

$$V_B = \frac{V_{in} \times 1\times10^{3}}{2\times10^{3}}$$

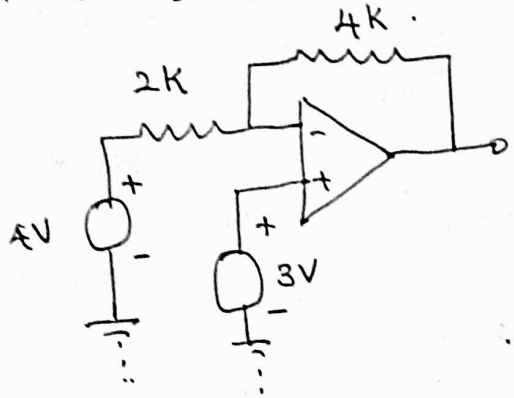
$$= \frac{V_{in}}{2} = \frac{10}{2} = 5V.$$

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_B$$

$$= 1 \left[\frac{50\times10^{3}}{10\times10^{3}}\right] 5$$

$$= 30V.$$

④ Find V_o for the following circuit :-



when 4V is acting, 3V is grounded, then it is inverting amplifier.

$$V_{o1} = -\left(\frac{R_f}{R_1}\right) V_{in} \quad \text{(Inverting)}.$$

$$= -\left(\frac{4}{2}\right) \times 4 = -8V.$$

when 3V is acting, 4V is grounded, it is non-inverting amplifier.

$$V_{o2} = \left(1 + \frac{R_F}{R_1}\right) \times 3 = \left(1 + \frac{4}{2}\right) \times 3.$$

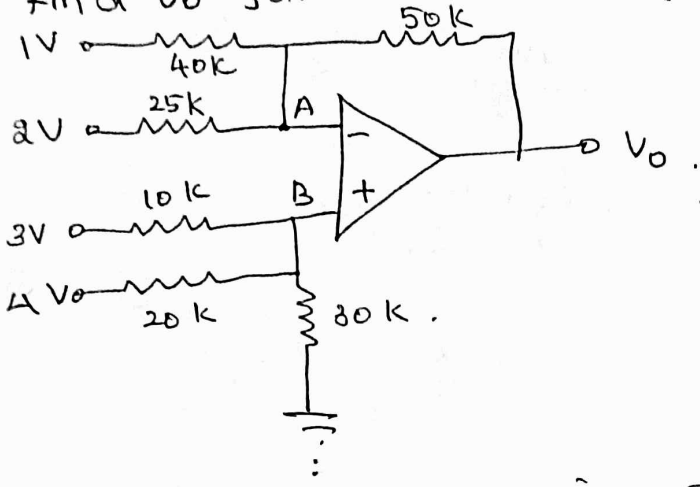
$$= 9V.$$

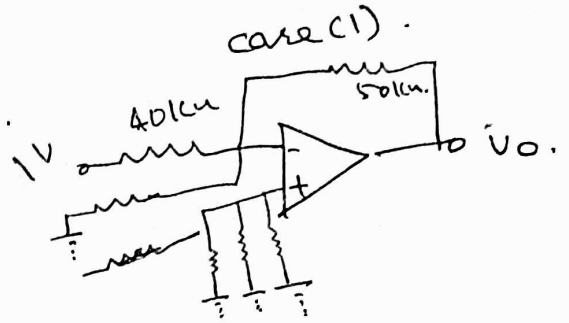
when 3V is acting, 4V is grounded. (It acts as non-inverting amplifier.

V_{02} = 1 + R

$V_o = V_{01} + V_{02} = -8 + 9 = 1V.$

⑤ Find V_o for the following circuit :-





case:1 1V is acting, all the sources grounded.

Node B is grounded, node A is virtual ground.

25 kΩ does not carry any current.

$V_{01} = -\left(\frac{R_F}{R_1}\right) V_{in}$ (Inverting).

$= -\left(\frac{50}{40}\right) \times 1 = -1.25\ V.$

case2 2V is acting, all the sources are grounded

$V_{02} = -\left(\frac{50}{25}\right) \times 2 = -4\ V.$ (Inverting).

case3

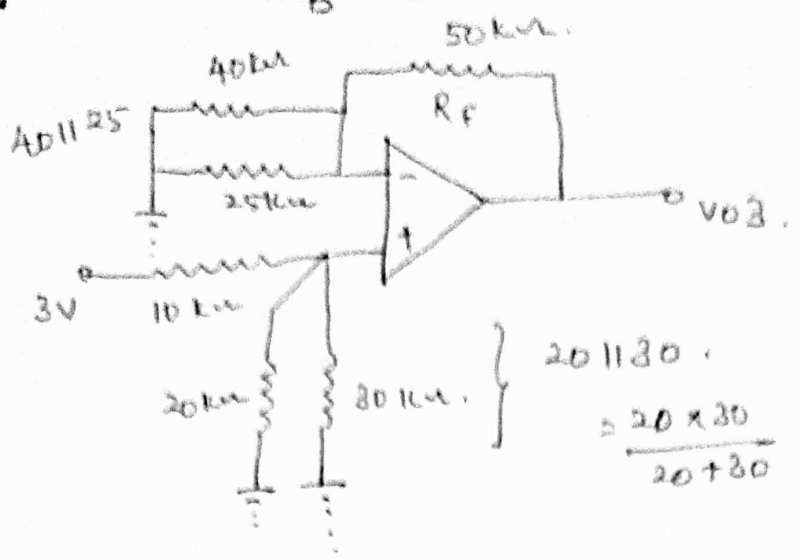
3V is acting, all the sources are grounded.

$R_{eq} = V_B = \left(\frac{R_3}{R_2 + R_3}\right) V_{in}.$

$R_1 = 25 \| 40 = \frac{25 \times 40}{25 + 40}$

$= 15.3846 k\Omega.$

V_B =



$20 \| 30$.

$= \frac{20 \times 30}{20+30} = 12\text{k}\Omega$.

$$V_B = \frac{R_2}{(R_2+R_3)} \times 3.$$

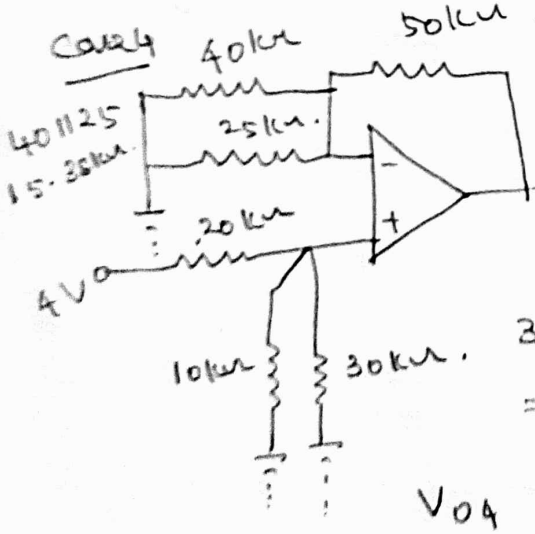
$$= \frac{12}{(10+12)} \times 3.$$

$$= 1.6363\ V.$$

$$V_{O3} = \left(1 + \frac{R_F}{R_1}\right) V_B.$$

$$= 6.9545\ V.$$

Case 4



$30 \| 10$

$= 7.5\text{k}\Omega$.

$$V_B = \frac{7.5}{(7.5+20)} \times 4.$$

$= 1.0909\ V.$

$$V_{O4} = V_B \left(1 + \frac{R_F}{R1}\right).$$

$$= 1.0909 \left(1 + \frac{50}{15.3846}\right).$$

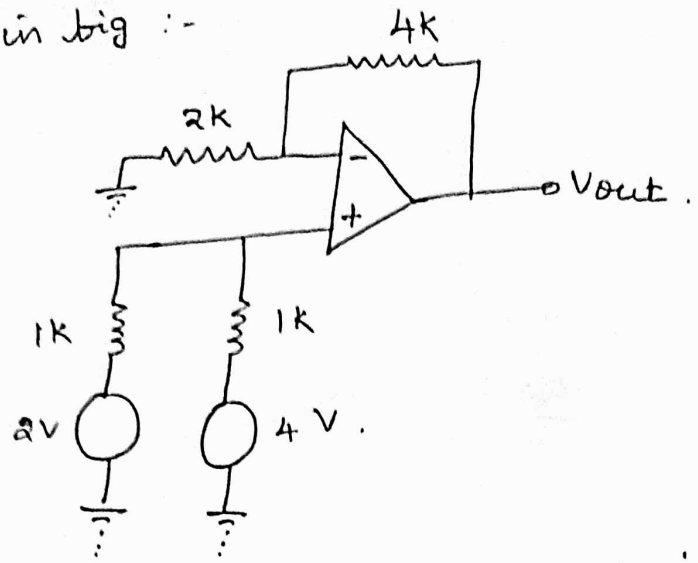
$$= 4.6363\ V.$$

$V_O = V_{O1} + V_{O2} + V_{O3} + V_{O4}$.

$= -1.85 - 4 + 6.9545 + 4.6363$.

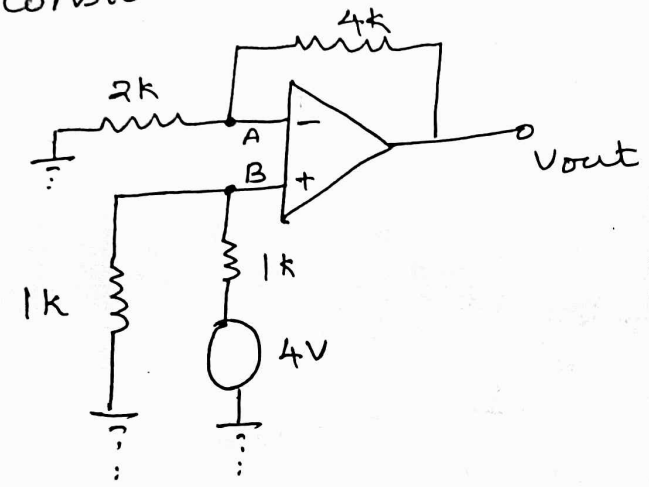
$= 6.3408\ V.$

① Determine the output voltage for the circuit shown in big :-



Solution :- use superposition principle.

consider 4V alone, short 2V.



$R_f = 4k.$

$R_1 = 2k.$

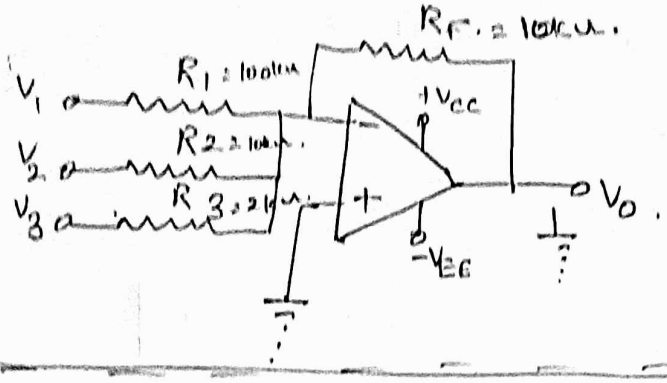
$$V_B = \frac{1\,k\Omega}{(1\,k\Omega + 1k\Omega)} \times 4V. \quad \text{[use potential divider rule]}.$$

$$= \frac{4}{2} = 2\,V.$$

$$V_{01} = \left[1 + \frac{R_f}{R_1}\right] V_B.$$

$$= \left[1 + \frac{4}{2}\right] \times 2\,V.$$

$$\boxed{V_{01} = 6\,V}$$



(3) Design a op-amp circuit to give an output

$V_o = V_1 - 2V_2 + 2V_3 - 3V_4$.

Soln The +ve & -ve terms can be added separately using two adders and then subtractor used.

Choose $R_{F1} = 100k\Omega$; For $V_1 + 2V_3$.

$$V_{01} = -\left[\frac{R_F}{R_1} V_1 + \frac{R_F}{R_3} V_3\right].$$

$\frac{R_F}{R_1} = 1$; $\frac{R_F}{R_3} = 2$.

$100k\Omega = R_1$; $\frac{100}{2} = R_3 \Rightarrow R_3 = 50k\Omega$.

$\boxed{R_1 = 100k\Omega ; R_3 = 50k\Omega} \Rightarrow V_{01} = -V_1 - 2V_3$.

For $-2V_2 - 3V_4$, choose $R_{F2} = 120k\Omega$.

$$V_{02} = -\left[\frac{R_F}{R_2} V_2 - \frac{R_F}{R_4} V_4\right].$$

$\frac{R_F}{R_2} = 2$; $\frac{R_F}{R_4} = -3$.

$\frac{120}{2} = R_2$; $\frac{120}{3} = R_4$.

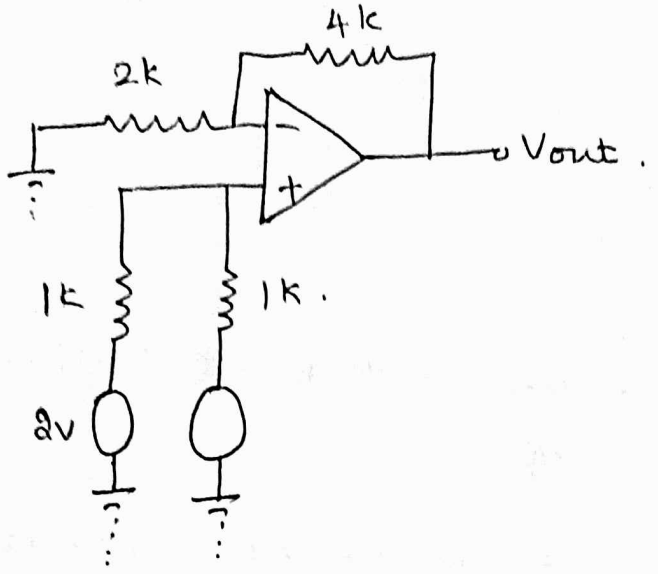
$\boxed{R_2 = 60k\Omega ; R_4 = 40k\Omega} \Rightarrow V_{02} = -2V_2 - 3V_4$.

The output of subtractor is $V_o = V_{02} - V_{01}$.

$V_o = (-2V_2 - 3V_4) - (-V_1 - 2V_3)$.

$\boxed{V_o = V_1 - 2V_2 + 2V_3 - 3V_4}$.

Now consider 2V source, Short 4V.



$$V_B = \frac{1k\Omega}{1k\Omega+1k\Omega} \times 2V.$$

$$= \frac{2}{2} = 1V.$$

$$V_{o2} = \left(1+\frac{R_F}{R_1}\right) V_B = \left(1+\frac{4}{2}\right) \times 1.$$

$$= 3V.$$

$$V_{out} = V_{o1} + V_{o2} = 6V + 3V = 9V.$$

---

② Draw an adder circuit for the given expression $V_o = -(0.1V_1 + V_2 + 5V_3)$.

$$V_o = -(0.1V_1 + V_2 + 5V_3).$$

$$= -\left[\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_3} V_3\right].$$

Choose $R_F = 10k\Omega$,

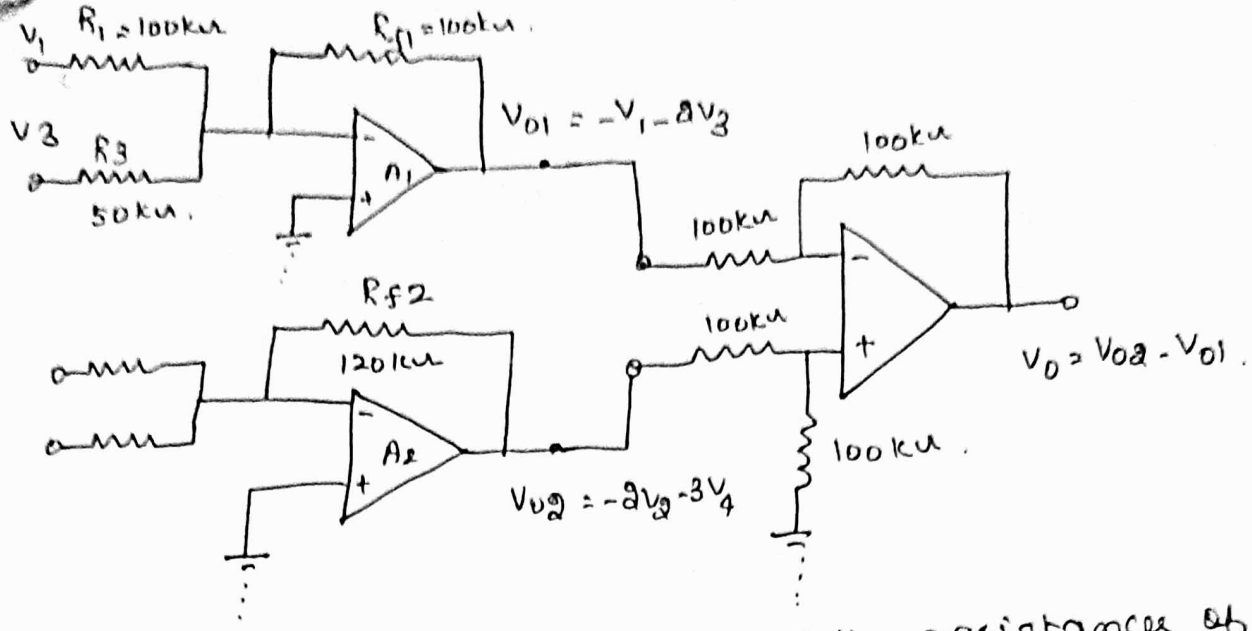
$$V_o = -\frac{R_F}{R_1} V_1.$$

$$\frac{R_F}{R_1} = 0.1 \; ; \; \frac{R_F}{R_2} = 1 \; ; \; \frac{R_F}{R_3} = 5.$$

$$\frac{10}{0.1} = R_1 \; ; \; \frac{10}{1} = R_2 \; ; \; \frac{10}{5} = R_3.$$

$$R_1 = 100k\Omega, \; R_2 = 10k\Omega, \; R_3 = 2k\Omega.$$

The designed circuit is,



use the subtractor with all the resistances of same value R = 100kΩ.

---

④ Design an adder - subtractor circuit for

$V_o = 2V_1 + 5V_2 - 10V_3$.

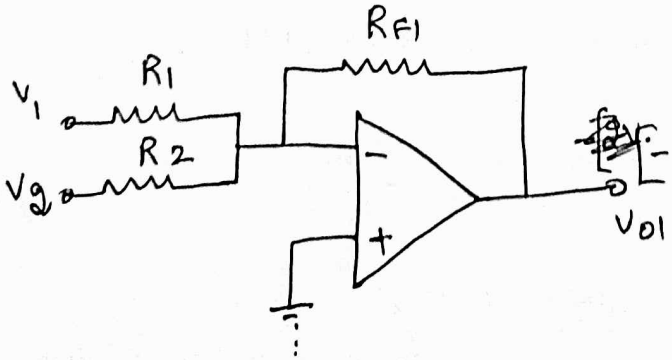
Step① Design adder to get $2V_1 + 5V_2$.

$$V_{01} = -\left[\frac{R_{F1}}{R_1}V_1 + \frac{R_{F1}}{R_2}V_2\right] \quad \text{--- (1)}$$

$\frac{R_{F1}}{R_1} = 2$; $\frac{R_{F1}}{R_2} = 5$. $\therefore V_{01} = -2V_1 + 5V_2$.

Choose $R_{F1} = 50k\Omega$, so $\frac{50}{R_1} = 2 \Rightarrow R_1 = 25k\Omega$.

$\frac{50}{R_2} = 5 \Rightarrow R_2 = 10k\Omega$.



$[-2V_1 + 5V_2]$.

Generate $10V_3$ using inverting Amplifier.

$$V_{02} = -\frac{R_{F3}}{R3} \times V_3 = -10V_3.$$

$$\frac{R_{F3}}{R3} = 10 \Rightarrow R_{F3} = 10R_3.$$

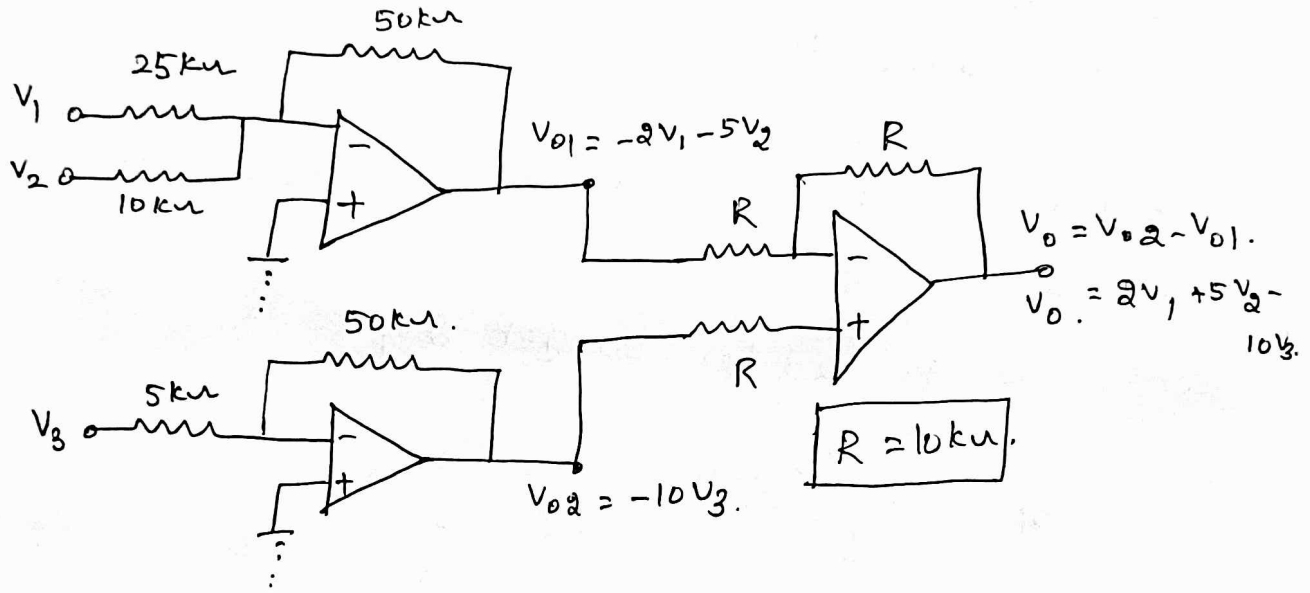
So $R_{F3} = 50k\Omega$, $R_3 = 5k\Omega$.

to get

use subtractor $V_0 = V_{02} - V_{01}$.

$$V_0 = -10V_3 - [-2V_1 - 5V_2].$$

$$= 2V_1 + 5V_2 - 10V_3.$$



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⑤ Design a practical Integrator circuit with a d.c gain of 10, to integrate a square wave of 10kHz.

d.c gain for the practical Integrator,

$$|A|_{d.c} = \frac{R_F}{R_1} \Rightarrow 10 = \frac{R_F}{R_1}.$$

The magnitude of the gain A is,

$$|A| = \frac{R_F/R_1}{\sqrt{1+\left(\frac{f}{f_a}\right)^2}}$$; at $f = 0$, d.c condition $|A|_{dc} = R_F/R_1$.

The input frequency $f = 10kHz$.

For proper integration, $f \geq 10 f_a$.

$f_a \rightarrow$ Break frequency of the practical Integrator.

$$\frac{f}{f_a} = 10.$$

$$f_a = \frac{f}{10} = \frac{10 \times 10^3}{10} = 1000Hz.$$

$$f_a = \frac{1}{2\pi R_F C_F}$$

$$1000 = \frac{1}{2\pi R_F C_F}.$$

Choose, $R_1 = 10k\Omega$, $R_F = 10 \times R_1 = 10 \times 10 = 100k\Omega$.

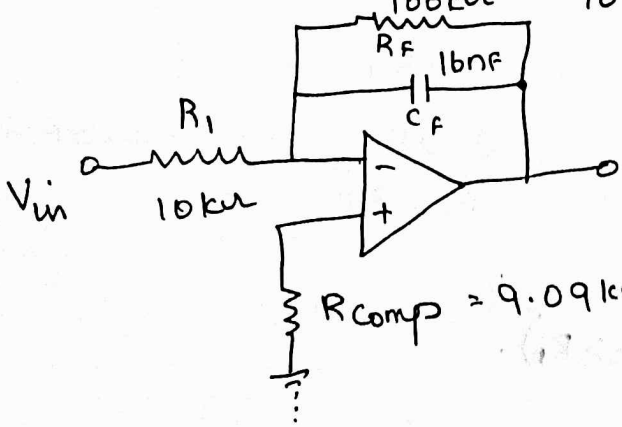
$$C_F = \frac{1}{2\pi R_F \times 1000}.$$

$$= \frac{1}{2\pi \times 1000 \times 100 \times 10^3}.$$

$$C_F = 1.5915 \times 10^{-9} \text{ (or) } 1.6nF.$$

$$R_{comp}' = R_1 \parallel R_F.$$

$$R_{comp} = \frac{10 \times 100}{10 + 100} = 9.09k\Omega.$$



(b) Design a practical differentiator circuit that will differentiate an input signal with the $f_{max} = 100$ Hz.

Soln

i) $f_a = f_{max} = 100$ Hz.

ii) Choose $C_1 = 0.1\mu F$.

$$f_a = \frac{1}{2\pi R_f C_1}.$$

$$100 = \frac{1}{2\pi R_f \times 0.1 \times 10^{-6}} \Rightarrow R_F = 15.91 k\Omega.$$

(iii) $f_b = 10 f_a$.

$= 10 \times 100 = 1000$ Hz.

$$f_b = \frac{1}{2\pi R_1 C_1}.$$

$$1000 = \frac{1}{2\pi R_1 \times 0.1 \times 10^{-6}}.$$

$$R_1 = 1.591 k\Omega.$$

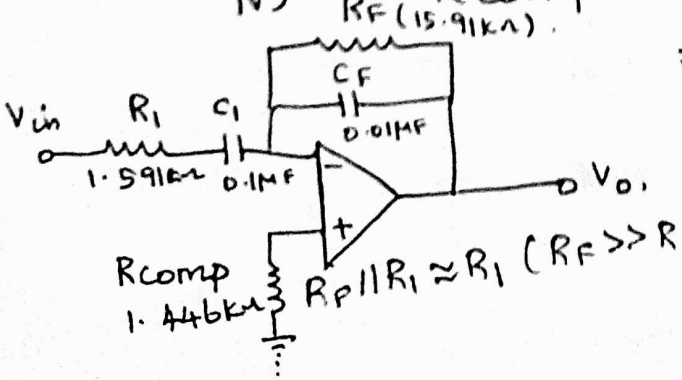
$$\boxed{R_1 C_1 = R_F C_F}. \quad ; \quad C_{F1} = 0.01\mu F.$$

$$C_F = \frac{R_1 C_1}{R_F} = \frac{1.591 \times 0.1}{15.91} \mu F$$

$$C_F = 0.01\mu F.$$

iv) $R_{comp} = R_1 \| R_F$.

$$= \frac{R_1 \times R_F}{R_1 + R_F} = 1.446 k\Omega.$$



$R_F \| R_1 \approx R_1$ ($R_F >> R_1$).

Steps to design practical Differentiator :-

① Choose f_a as the highest frequency of the input signal.

② Choose C_1 less than 1 μF, calculate R_F.

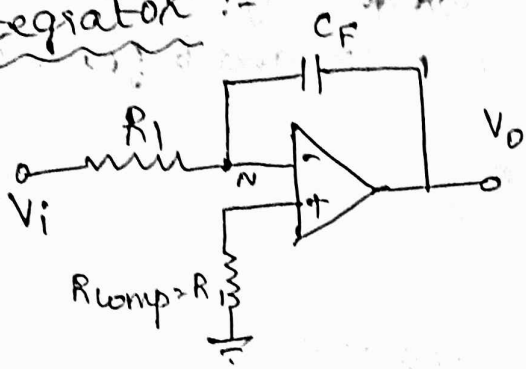
$$f_a = \frac{1}{2\pi R_F C_1}$$

③ Choose f_b as 10 times f_a which ensures $f_a < f_b$. $\quad f_b = \frac{1}{2\pi R_1 C_1}$

④ calculate R_1, C_F from $R_1 C_1 = R_F C_F$.

⑤ $R_{comp} = R_1 \| R_F$. practically equal to R_1.

Integrator :-



⇒ If we interchange the resistor and capacitor of the differentiator, integrator circuit is obtained.

The nodal equation at Node N

$$\frac{V_i}{R_1} + C_f \frac{dV_o}{dt} = 0.$$

$$\frac{dV_o}{dt} = -\frac{1}{R_1 C_f} V_i$$

Integrating both sides we get,

$$\int_0^t dV_o = -\frac{1}{R_1 C_F} \int_0^t V_i dt.$$

$$V_o(t) = -\frac{1}{R_1 C_F} \int_0^t V_i(t) dt + V_o(0).$$

$V_o(0)$ → initial output voltage.

⇒ o/p voltage proportional to the time integral of the input, R_1C_F → time constant of the integrator.

⇒ $R_{comp} = R_1$ connected to the (+) input terminal to minimize the effect of input bias current.

$$V_o(s) = -\frac{1}{sR_1C_F} V_i(s).$$

$$s = j\omega,$$

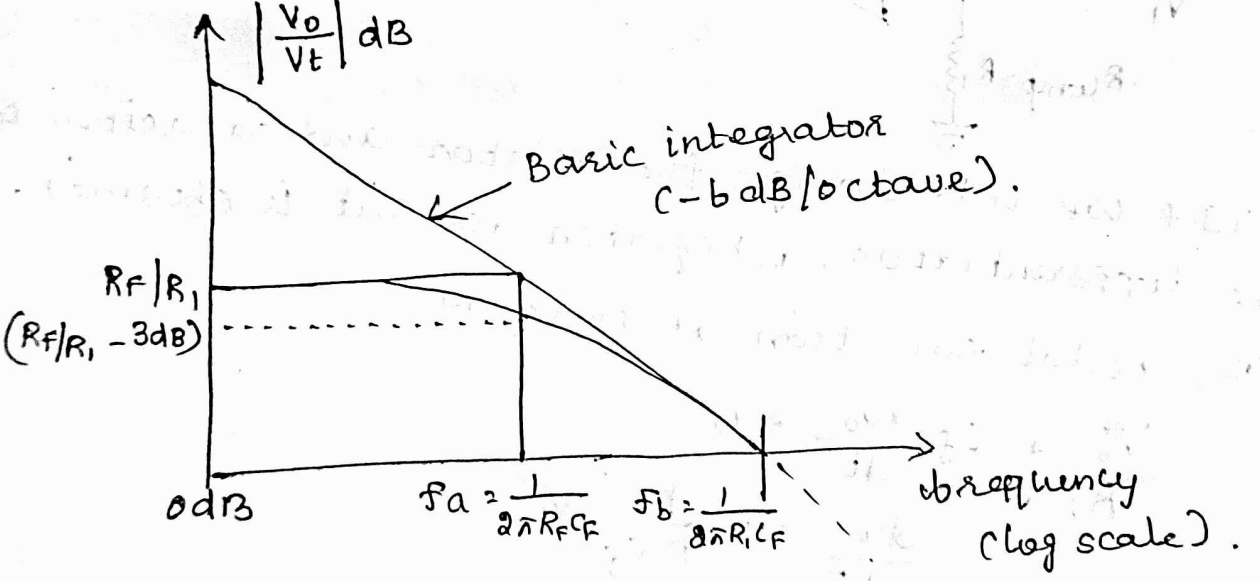
$$V_o(j\omega) = -\frac{1}{j\omega R_1 C_F} V_i(j\omega).$$

Magnitude of the gain $|A| = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \left|-\frac{1}{j\omega R_1 C_F}\right|$

$$= \frac{1}{\omega R_1 C_F}.$$

The frequency f_b is the frequency at which the gain of the integrator is 0 dB and is given by;

$$f_b = \frac{1}{2\pi R_1 C_F}$$



Frequency response of a basic and Lossy integrator.

UNIT - III

Applications of Op-amp.

Instrumentation Amplifiers and its applications for transducer Bridge, Log and Antilog Amplifiers, Analog multiplier & Divider, First and second order active filters, comparators, multivibrators, waveform generators, clippers, clampers, peak detector, S/H circuit, D/A Converter (R-2R ladder and weighted resistor types), A/D Converters using op-amps.

Instrumentation Amplifiers :-

The special Amplifier which is used for such a low level amplification with high CMRR, high input impedance to avoid loading, low power consumption and some other features is called an Instrumentation Amplifier.

It is also called data amplifier and is barically a difference Amplifier.

The expression for voltage gain is,

$$A = \frac{V_o}{V_2 - V_1}$$

V_o → output of the Amplifier.

$V_2 - V_1$ → Differential input which is to be amplified.

Requirements of a Good Instrumentation Amplifier

1) Finite, accurate and stable gain :-

As very low level signals are required to be amplified by the Instrumentation Amplifiers. The gain in the range of 1 to 1000. The gain has to be accurate and closed loop gain must be stable.

2) Easier gain adjustment :

The gain adjustment must be easier and precise. Gain adjustment is done using a Potentiometer or digitally with the help of switches which are JFET or MOSFET switches.

3) High input impedance :-

To avoid the loading of input sources, input impedance of the instrumentation Amplifier must be very high.

4) Low output impedance :-

Externally low output impedance (ideally zero) to avoid the loading.

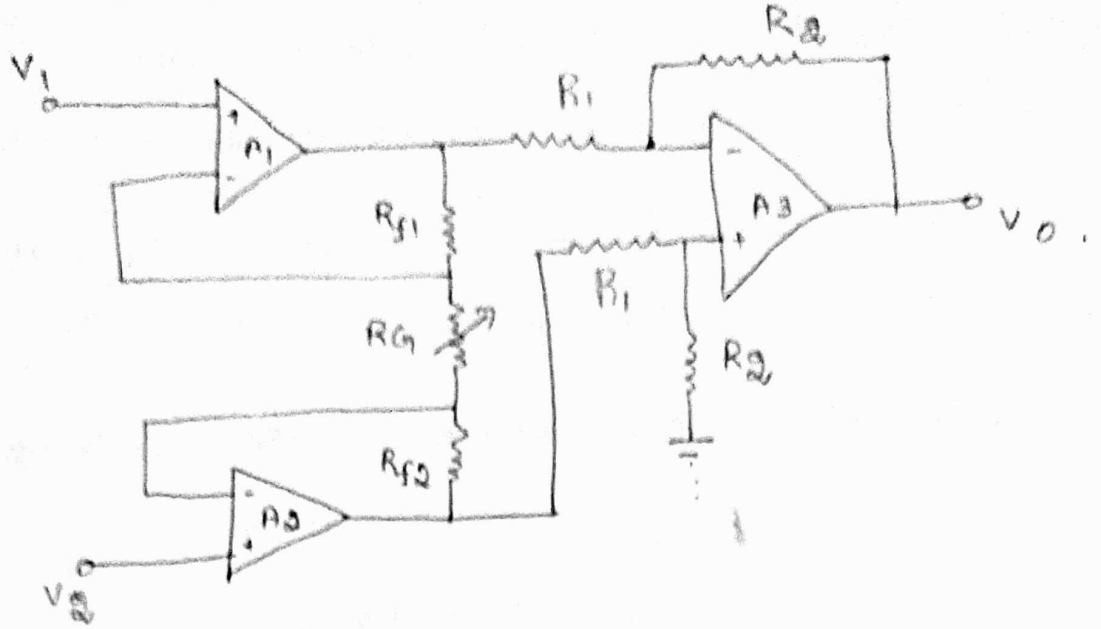
5) High CMRR.

6) Low power consumption.

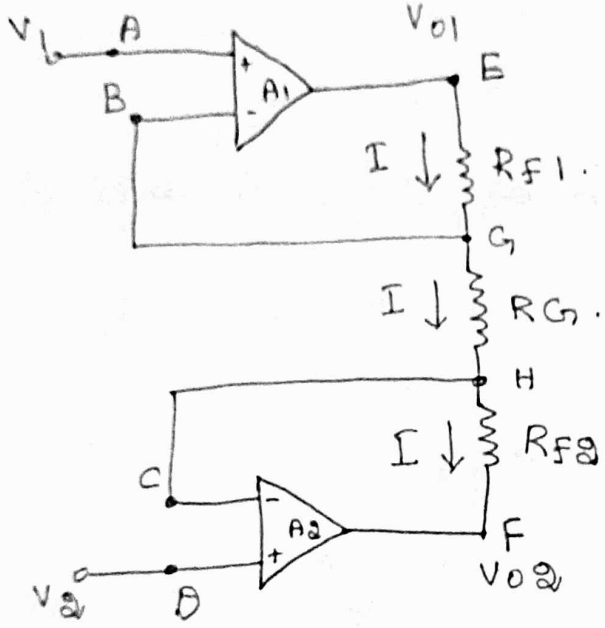
7) Low thermal and time drifts.

8) High slew rate.

Three op-amp Instrumentation Amplifier :-



Analysis of Three op-amp Instrumentation Amplifier :



The output of the op-amp A_1 is V_{01}.

output of the op-amp A_2 is V_{02}.

$$V_o = \frac{R_2}{R_1}(V_{02} - V_{01}) \quad \text{— (I)}.$$

The node A potential of op-amp A_1 is V_1.

Realistic Assumption, the potential of node B is also V_1. Potential of G is also V_1.

The node D potential of op-amp A_2 is V_2. From the realistic assumption, potential of node C is also V_2. Potential of H is also V_2

⇒ Input current of op-amp A_1, A_2 both are 0

I remains same through R_{f1} R_G R_{f2}.

Apply ohm's law between nodes E and F,

$$I = \frac{V_{o1} - V_{o2}}{R_{f1} + R_G + R_{f2}} \quad \text{— (1)}$$

Let $R_{f1} = R_{f2} = R_f$.

$$I = \frac{V_{o1} - V_{o2}}{2R_f + R_G} \quad \text{— (2)}$$

observation of nodes G and H,

$$I = \frac{V_G - V_H}{R_G} = \frac{V_1 - V_2}{R_G} \quad \text{— (3)}$$

Equate (2) & (3),

$$\frac{V_{o1} - V_{o2}}{2R_f + R_G} = \frac{V_1 - V_2}{R_G}$$

$$\frac{V_{o2} - V_{o1}}{2R_f + R_G} = \frac{V_2 - V_1}{R_G}$$

$$V_{o2} - V_{o1} = \frac{(2R_f + R_G)(V_2 - V_1)}{R_G} \quad \text{— (4)}$$

sub (4) in (1),

$$V_o = \frac{R_2}{R_1}\left[\frac{(2R_f + R_G)(V_2 - V_1)}{R_G}\right]$$

overall gain of circuit

$$\boxed{V_o = \frac{R_2}{R_1}\left[1 + \frac{2R_f}{R_G}\right][V_2 - V_1]}$$

Advantages :-

1) Due to variable resistance R_G, the gain can be easily varied.

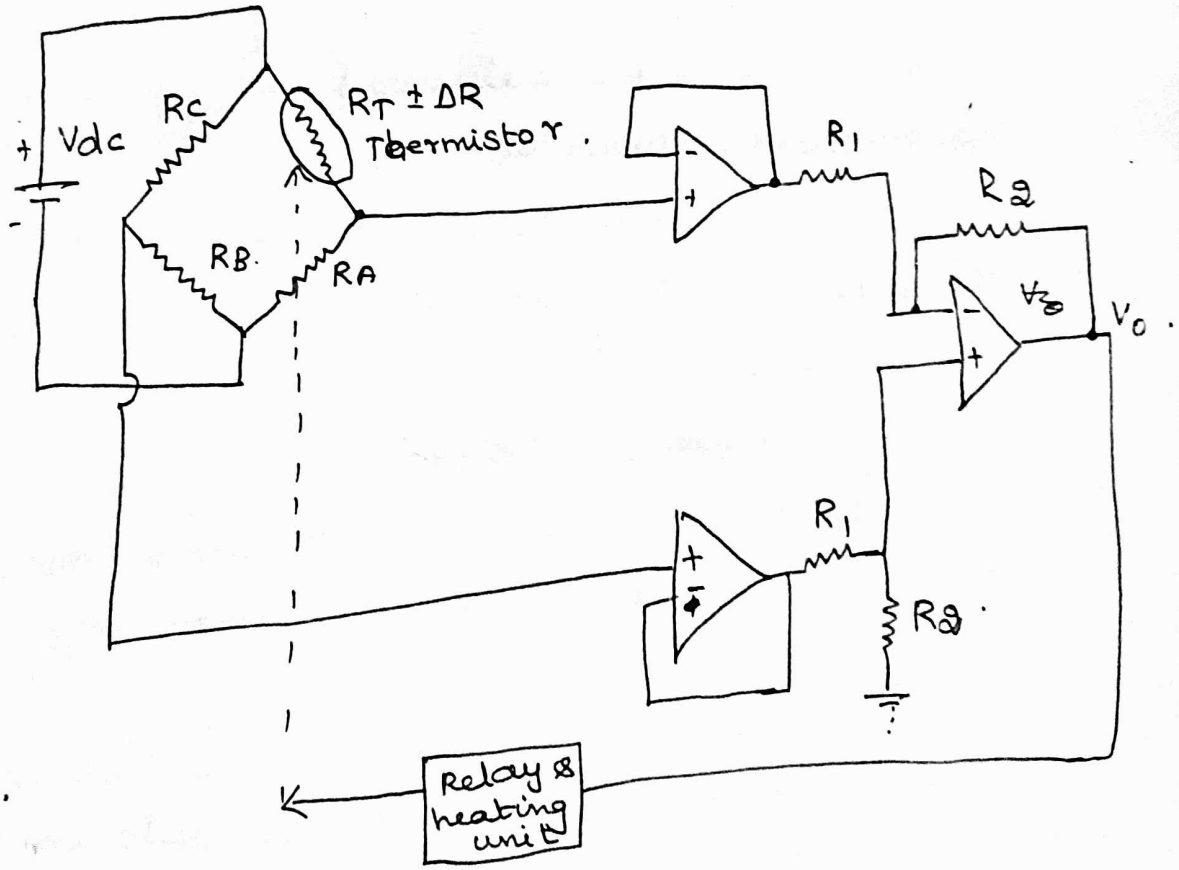
2) The input impedance depends on the input impedance of non-inverting amplifiers which is high.

3) The output impedance of the op-amp A_3 which is very very low.

4) The CMRR of the op-amp A_3 is very high.

Applications :-

1) Temperature controller :-



simple temperature controller.

=) A simple temperature control circuit can be constructed using thermistor in the transducer bridge.

=) The bridge is set balanced for a particular reference temperature.

=) Any change in this temperature, the instrumentation Amplifier produces the output voltage.

=) This voltage used to drive the relays which inturn controls the ON-OFF of the heating unit to control temperature.

(2) Temperature Indicator :-

=) The same circuit used as temperature Indicator.

=) Bridge is kept balanced at some reference temperature when $V_o = 0$ V.

=) The meter connected at the output is calibrated. As temp changes, amplifier output also changes.

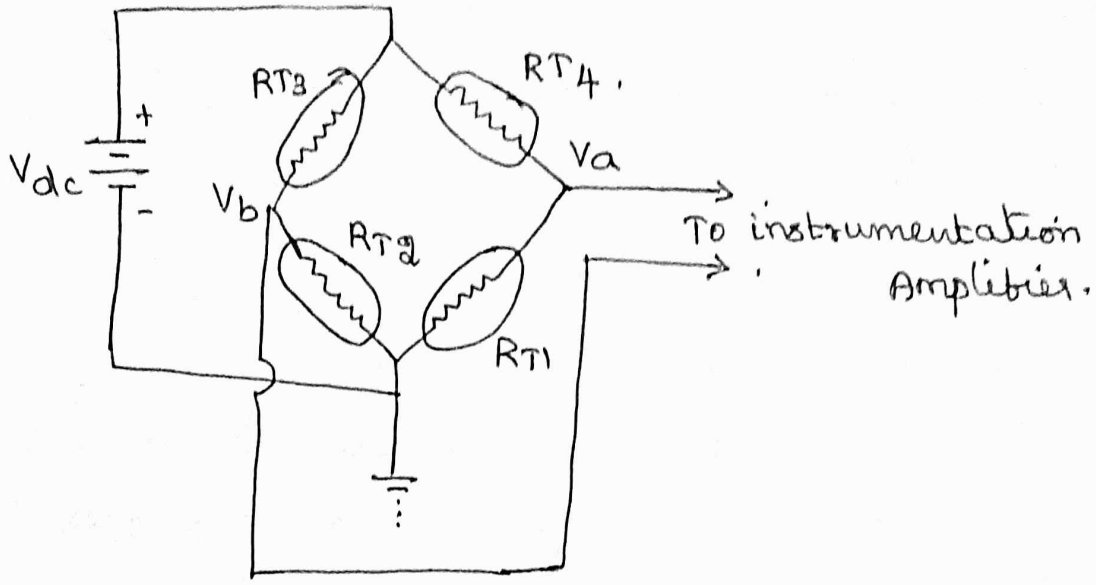
(3) Light intensity Meter :-

=) In the same circuit thermistor replaced with a photocell used as a simple light intensity meter.

=) The bridge is made balanced for the darkness condition. When light falls on the photocell its resistance changes and produces unbalanced bridge conditon.

=) This produces the output, which inturn produces the meter deflection.

Analog weight scale :-



=> Strain gauges are used in all the four arms of the bridge can be used as a simple analog weight scale.

=> The elements are mounted on the base of the weight platform.

=> When the weight is placed on the platform the strain gauges in the opposite arm elongate while the strain gauges in other two opposite arms get compressed.

R_{T1}, R_{T3} decreases. R_{T2}, R_{T4} increases.

under no weight on the platform, the bridge is balanced $R_{T1} = R_{T2} = R_{T3} = R_{T4} = R$. Bridge output is 0 V.

Unbalanced Condition, the change in Resistance is ΔR ohms. Increase of ΔR for R_{T2}, R_{T4},

Decrease of ΔR for R_{T1}, R_{T3}.

$$V_b = \frac{(R+\Delta R)V_{dc}}{R-\Delta R+R+\Delta R} = \frac{(R+\Delta R)V_{dc}}{2R}$$

$$V_a = \frac{(R-\Delta R)V_{dc}}{(R-\Delta R+R+\Delta R)} = \frac{(R-\Delta R)V_{dc}}{2R}$$

$$V_{ab} = V_b - V_a = \frac{(R+\Delta R)V_{dc}}{2R} - \frac{(R-\Delta R)V_{dc}}{2R}$$

$$= \frac{2\Delta R V_{dc}}{2R} = \frac{\Delta R V_{dc}}{R}$$

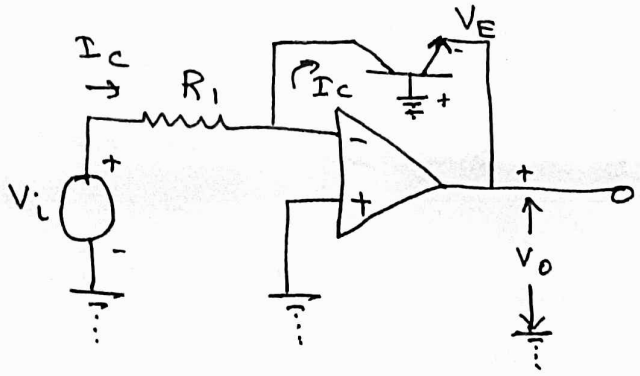
Net output voltage is,

$$\boxed{V_o = A\frac{\Delta R V_{dc}}{R}}$$

Log and Antilog Amplifier :-

=> To have direct dB display on digital voltmeter and spectrum analyser, Log amplifier used to perform this function.

=> Log amplifier used to compress the dynamic range of a signal.



Fundamental log Amp circuit.

=> A grounded base transistor is placed in the feedback path. Collector is held at virtual ground and the base is also grounded.

=> The transistor's voltage-current relationship becomes that of a diode.

$$I_E = I_S\left(e^{qV_E/KT} - 1\right).$$

$I_C = I_E$ for a grounded base Transistor.

$$I_C = I_S\left[e^{qV_E/KT} - 1\right].$$

where I_S = Emitter Saturation current
$= 10^{-13}$ A.

k = Boltzmann's Constant.

T = Absolute temperature (in °K).

$$\frac{I_C}{I_E} \quad \frac{I_C}{I_S} = (e^{qV_E/kT} - 1).$$

$$e^{qV_E/kT} = \frac{I_C}{I_S} + 1.$$

$$e^{qV_E/kT} = \frac{I_C}{I_S} \quad [I_S = 10^{-13} A,\ I_C >> I_S].$$

Taking natural log on both sides,

$$\ln\left[e^{qV_E/kT}\right] = \ln \frac{I_C}{I_S}.$$

$$qV_E/kT = \ln \frac{I_C}{I_S}.$$

$$V_E = \frac{kT}{q} \ln\left[\frac{I_C}{I_S}\right].$$

$$I_C = \frac{V_i}{R_1}$$

$$V_E = -V_o.$$

$$-V_o = \frac{kT}{q} \ln\left[\frac{V_i}{R_1 I_S}\right].$$

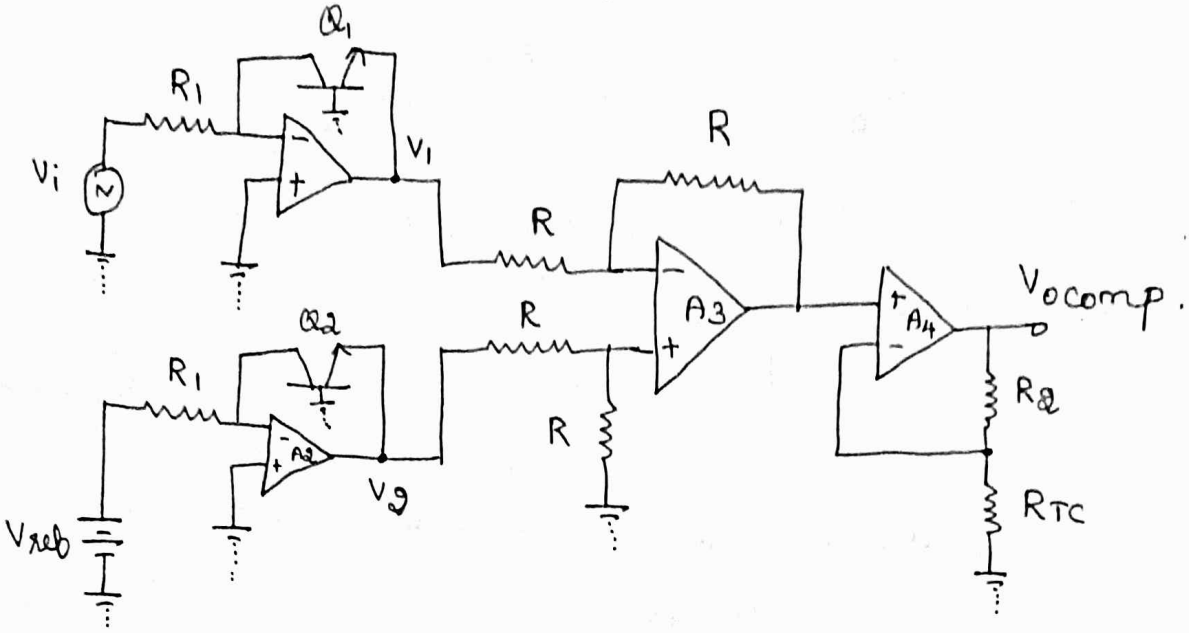
$$V_o = \frac{-kT}{q} \ln\left[\frac{V_i}{V_{ref}}\right].$$

where $V_{ref} = R_1 I_S$.

$$\log_{10} x = 0.4343 \ln x.$$

⇒ The emitter saturation current I_S varies from transistor to transistor and with temperature So, stable reference voltage V_{ref} cannot be obtain

This is eliminated by the circuit.



Log amplifier with saturation current and temperature compensation.

Assume, $I_{S1} = I_{S2} = I_S$.

$$V_1 = \frac{-KT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right).$$

$$V_2 = \frac{-KT}{q} \ln\left(\frac{V_{ref}}{R_1 I_S}\right).$$

$$V_o = V_2 - V_1 = \frac{-KT}{q}\left\{\ln\left(\frac{V_{ref}}{R_1 I_S}\right) - \left[\frac{-KT}{q}\ln\left(\frac{V_i}{R_1 I_S}\right)\right]\right.$$

$$= \frac{KT}{q}\left[-\ln\left(\frac{V_{ref}}{R_1 I_S}\right) + \ln\left(\frac{V_i}{R_1 I_S}\right)\right].$$

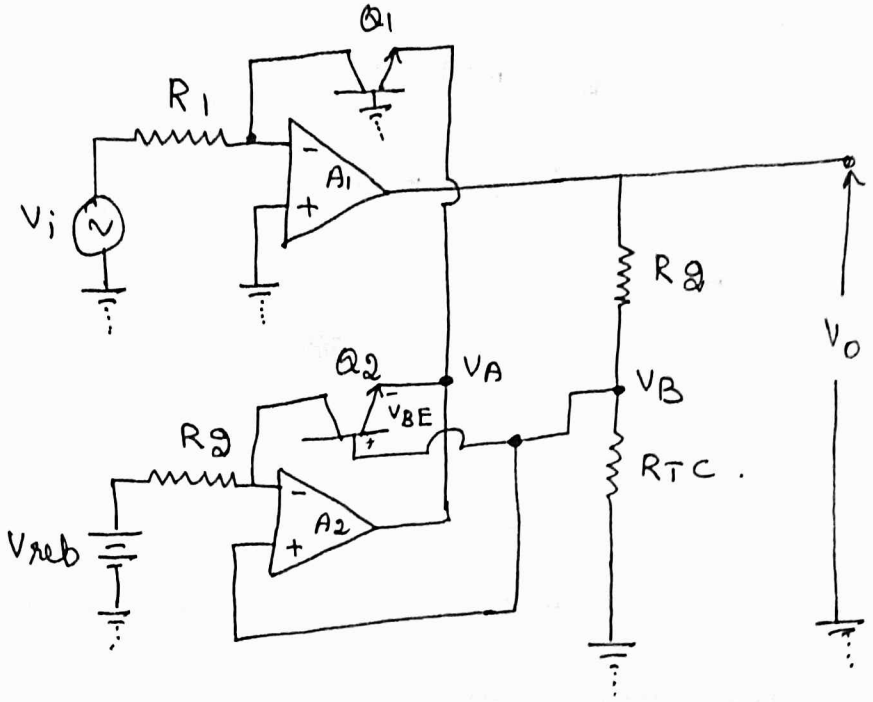
$$= \frac{KT}{q}\left[\ln\left(\frac{V_i}{R_1 I_S}\right) - \ln\left[\frac{V_{ref}}{R_1 I_S}\right]\right].$$

$$V_o = \frac{KT}{q}\left[\ln \frac{\frac{V_i}{R_1 I_S}}{\frac{V_{ref}}{R_1 I_S}}\right] = \frac{KT}{q}\left[\ln \frac{V_i}{V_{ref}}\right].$$

Reference level Vref is now set.
Vo dependent upon temperature and directly proportional to T. The op-amp A_4 provides a non-inverting gain of $1 + \frac{R_2}{R_{TC}}$.

$$V_{o\,comp} = \left(1 + \frac{R_2}{R_{TC}}\right) \frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right).$$

=> The circuit is expensive. requires 4 op-amps.
The same circuit obtained using two op-amps.



Log amplifier using two-op-amps only.

Antilog Amplifier :-

=> The input Vi for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2.

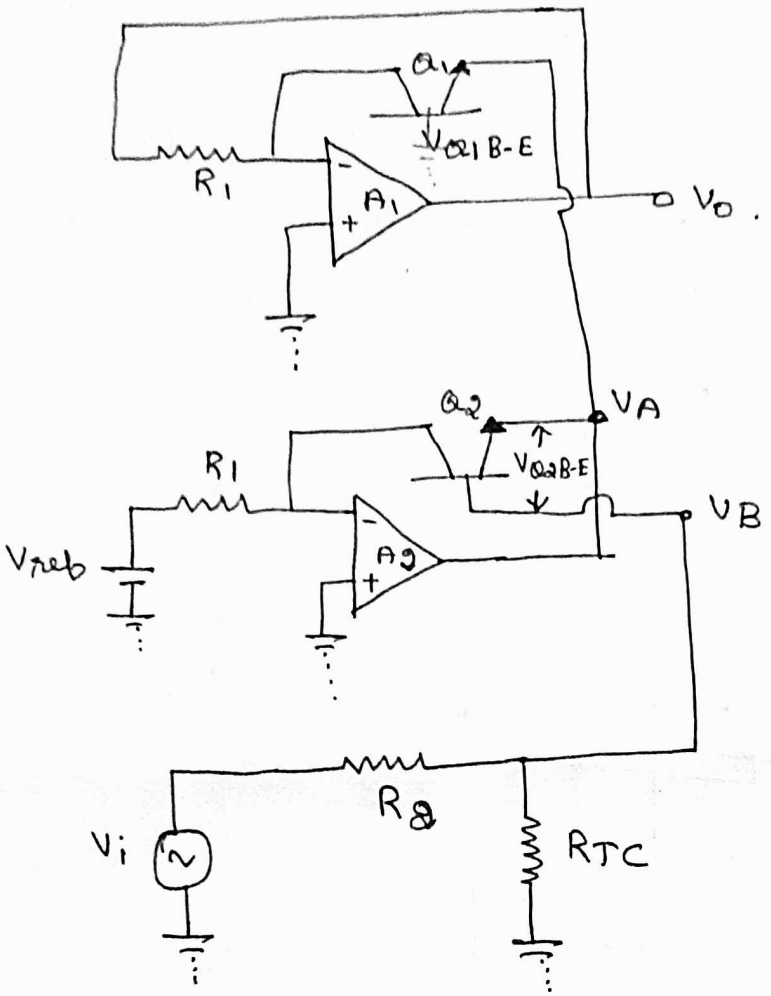
=> The output Vo of the antilog amp is fed back to the inverting input of A_1 through Resistor R_1.

$$V_{Q_1,\,B\text{-}E} = \frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_S}\right).$$

$$V_{Q_2\,B-E} = \frac{kT}{q} \ln\left(\frac{V_{reb}}{R_1 I_S}\right).$$

Since the base of Q_1 is tied to ground,

$$V_A = -V_{Q_1\,B-E} = -\frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_S}\right).$$



Antilog Amplifier.

The base voltage V_B of Q_2 is,

$$V_B = \left[\frac{R_{TC}}{R_Q + R_{TC}}\right] V_i$$

The voltage at the emitter of Q_2 is,

$$V_{Q_2\,B-E} = V_B + V_{Q_2\,E-B}.$$

$$V_{Q_2\,B-E} = \left(\frac{R_{TC}}{R_Q + R_{TC}}\right) V_i - \frac{kT}{q} \ln\left(\frac{V_{reb}}{R_1 I_S}\right).$$

Emitter voltage of Q_2 is V_A,

$$V_A = -V_{Q_1\,B-E}.$$

$$-\frac{kT}{q} \ln\frac{V_o}{R_1 I_S} = \left(\frac{R_{TC}}{R_Q + R_{TC}}\right) V_i - \frac{kT}{q} \ln\left(\frac{V_{reb}}{R_1 I_S}\right).$$

$$\frac{R_{TC}}{R_2 + R_{TC}} V_i = -\frac{KT}{q}\left[\ln \frac{V_o}{R_1 I_S} - \ln \frac{V_{reb}}{R_1 I_S}\right].$$

$$-\frac{q}{KT} \times \frac{R_{TC}}{R_2 + R_{TC}} V_i = \ln\left[\frac{V_o}{V_{reb}}\right].$$

changing natural log

change ln to $\log_{10}$.

$$-0.4343\left(\frac{q}{KT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right] V_i = 0.4343 \times \ln\left(\frac{V_o}{V_{reb}}\right)$$

$$-K' V_i = \log_{10}\left(\frac{V_o}{V_{reb}}\right).$$

where $K' = 0.4343\left(\frac{q}{KT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$.

$$10^{-K' V_i} = \frac{V_o}{V_{reb}}.$$

$$V_o = V_{reb}\left(10^{-K' V_i}\right).$$

755 log/antilog amplifier IC chip is available.

Analog Multiplier :-

Applications :-

(i) Frequency doubling.

(ii) Measurement of real power.

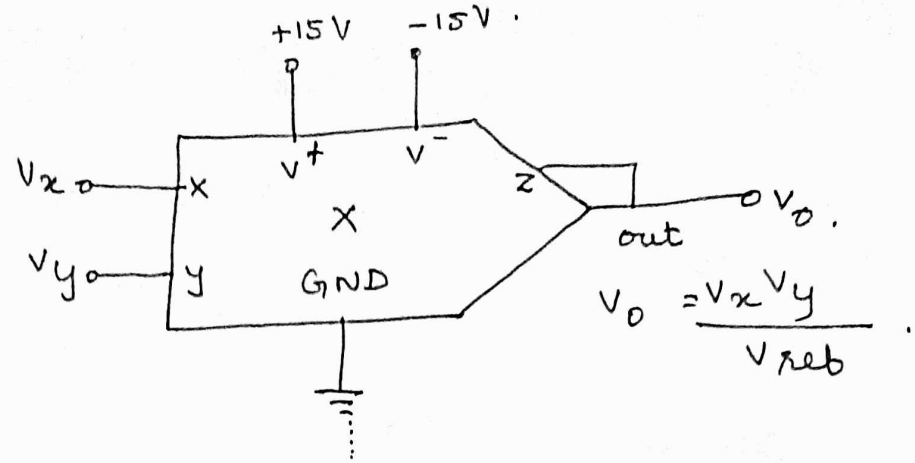
iii) Detecting phase-angle difference between two signals of equal frequency.

(iv) Multiplying two signals.

v) Dividing one signal by another.

vi) Taking square root of a signal.

vii) Squaring a signal.



Multiplier Symbol.

Two signal inputs (V_x, V_y) are provided. The output is the product of the two inputs divided by a reference voltage V_{reb}.

$$V_o = \frac{V_x V_y}{V_{reb}}$$

Internally V_{reb} is set to 10 Volt.

$$V_o = \frac{V_x V_y}{10}$$

As long as,

$$V_x < V_{reb}.$$

$$V_y < V_{reb}.$$

Power supply voltage can range from ±8V to ±18V. usually power supplies used for ±15 V.

=> Both inputs are positive, Ic → one Quadrant Multiplier

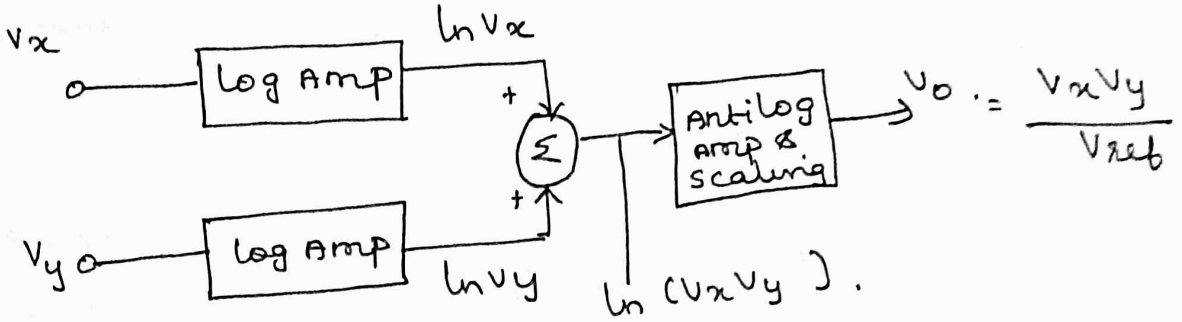
=> one input is +ve, the other is allowed to swing both +ve & -ve, → Two Quadrant Multiplier.

=> If both inputs either +ve or -ve, Ic → Four Quadrant multiplier.

Log - antilog method :-

$$\ln V_x + \ln V_y = \ln (V_x V_y).$$

sum of the logarithm of two numbers equals the logarithms of the product of those numbers.



Multiplier IC chips are AD 533, AD534, AD633.

Frequency Doubling :-

Let $V_x = V_x \sin \omega t$

$V_y = V_y \sin(\omega t + \theta)$.

$\theta \rightarrow$ phase difference between two signals.

$$V_o = \frac{V_x V_y}{V_{ref}}$$

$$V_o = \frac{V_x \sin \omega t \; V_y \sin(\omega t + \theta)}{V_{ref}}$$

$$V_o = \frac{V_x V_y}{V_{ref}} \sin \omega t (\sin \omega t \cos\theta + \sin\theta \cos \omega t).$$

$$= \frac{V_x V_y}{V_{ref}} (\sin^2 \omega t \cos\theta + \sin\theta \sin \omega t \cos \omega t).$$

$\sin^2 \alpha = 1 - \cos^2 \alpha$. — (1)

$\cos^2 \alpha = 2\cos^2 \alpha - 1$. — (2)

$\cos^2 \alpha = \frac{1}{2}\cos 2\alpha + 1$. $\cos^2 \alpha = 1 + \frac{\cos 2\alpha}{2}$

$\cos^2 \alpha = \frac{1}{2} + \frac{1}{2}\cos 2\alpha$. — (3)

$= \frac{\cos^2 \alpha + 1}{2}$

sub ④ in ①

$$\sin^2 a = 1 - \frac{1}{2} - \left(\frac{1}{2}\right)\cos 2a.$$

$$= \frac{1}{2} - \frac{1}{2}\cos 2a.$$

$$V_0 = \frac{V_x V_y}{V_{reb}}\left[\cos\alpha\left(\frac{1}{2} - \left(\frac{1}{2}\right)\cos 2\omega t\right) + \sin\alpha \sin\omega t \cos\omega t\right].$$

$$\sin a \cos a = \frac{\sin 2a}{2}.$$

$$V_0 = \frac{V_x V_y}{2 V_{reb}}\left[\cos\alpha - \cos\alpha\cos 2\omega t + \sin\alpha \sin 2\omega t\right].$$

$$V_0 = \frac{V_x V_y}{2 V_{reb}}\cos\alpha + \frac{V_x V_y}{2 V_{reb}}\left[\sin\alpha\sin 2\omega t - \cos\alpha\cos 2\omega t\right]$$

The circuit works as an ideal doubler, if same frequency is applied to both the inputs.

$$V_x = V_x \sin\omega t$$

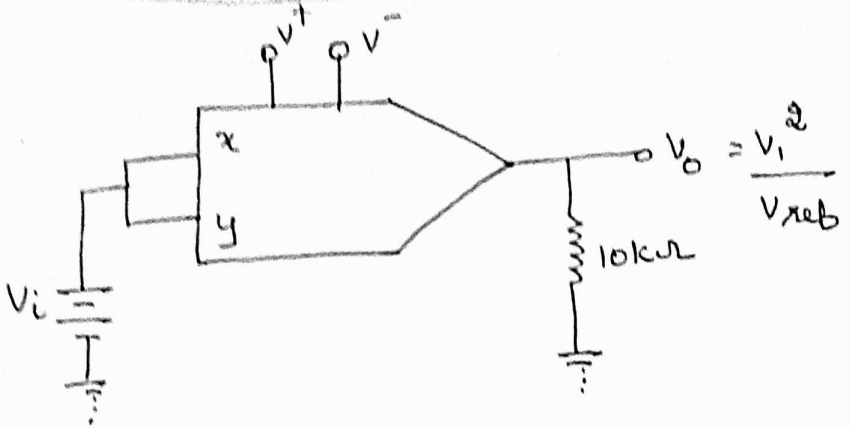
$$V_y = V_y \sin\omega t.$$

$$V_0 = \frac{V_x V_y}{V_{reb}} \sin^2\omega t.$$

$$V_0 = \frac{V_x V_y}{V_{reb}}\left[1 - \frac{\cos 2\omega t}{2}\right].$$

The output contains a dc term and a negative cosine wave of double frequency. It is removed by using a 1 MF coupling capacitor between load and the output terminal.

Squarer circuit :-



Squarer circuit

Baric multiplier can be used to square any +ve or -ve number. The number represented by a voltage between 0 to V_{ref}.

⇒ V_i representing the number is connected to both the inputs.

⇒ It is possible to square a sinewave voltage too.

⇒ Sinewave voltage $V_i = V_m \sin \omega t$ is applied to both the inputs.

$$V_o = \frac{V_i^2}{V_{ref}}.$$

$$\left.\begin{aligned} V_i &= 5 \sin 2\pi \times 10^4 t \\ V_{ref} &= 10\ V. \end{aligned}\right\} \text{ Given}$$

$$V_o = \frac{5^2 \left(5 \sin 2\pi \times 10^4\right)^2}{10}$$

$$= 2.5 \left[\frac{1}{2} - \frac{1}{2} \cos 2\pi \times 2 \times 10^4 t\right].$$

$$= \frac{2.5}{2} - \frac{2.5}{2} \cos 2\pi \times 2 \times 10^4 t.$$

$$= 1.25 - 1.25 \cos 2\pi \times 2 \times 10^4 t.$$

The output contains dc term and Frequency is doubled.

Phase angle Detection :-

The two input signals applied to a multiplier are

$$V_x = V_{mx} \sin \omega t.$$

$$V_y = V_{my} \sin(\omega t + \theta).$$

$$V_o = \frac{V_{mx} V_{my}}{V_{ref}} \sin \omega t \sin(\omega t + \theta).$$

$$= \frac{V_{mx} V_{my}}{V_{ref}} \times \frac{\cos\theta - \cos(2\omega t + \theta)}{2}$$

$$\boxed{V_{o,dc} = \frac{V_{mx} V_{my}}{2 V_{ref}} \times \cos\theta}$$

The phase difference θ between the two input signals can be calculated from the dc component in the output voltage V_o.

Divider :-

Division, the complement of multiplication can be accomplished by placing the multiplier circuit in the op-amp's feedback loop.

Input signals V_z & V_x as dividend and divisor respectively.

$$V_o = -V_{ref} \frac{V_z}{V_x}.$$

The op-amp's inverting terminal is at virtual ground.

$$I_z = I_A.$$

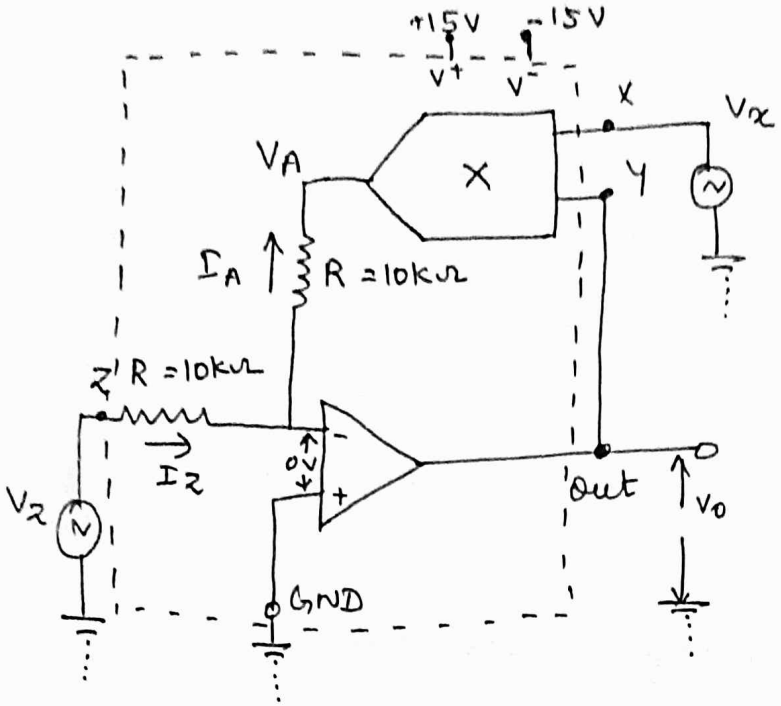
$$I_z = \frac{V_z}{R}.$$

$$V_A = \frac{V_x V_y}{V_{ref}} = \frac{V_x V_o}{V_{ref}}.$$

$$V_A = -I_A R.$$

$$I_A = -\frac{V_A}{R}$$

$$= -\frac{V_x V_o}{V_{reb} R}$$



Multiplier IC configured as divider.

$$I_z = I_A$$

$$I_z = -\frac{V_x V_o}{V_{reb} R}$$

$$V_z = I_z R = -\frac{V_x V_o}{V_{reb} R} \times R = -\frac{V_x V_o}{V_{reb}}$$

$$V_o = -V_{reb} \frac{V_z}{V_x}.$$

To find square Roots :-

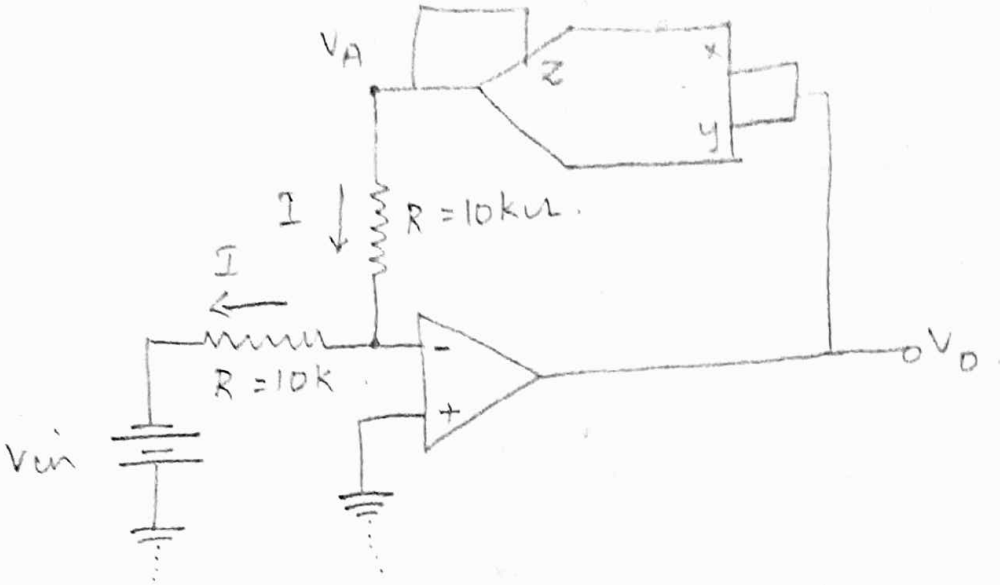
A divider circuit used to find square roots by connecting both the inputs of the multiplier to the output of an op-amp.

$$V_A = \frac{V_o}{V_{reb}} \quad \& \quad V_A = -V_{in}$$

$$V_o = -V_{in} \cdot V_{reb}.$$

$$V_o = \sqrt{V_{reb} \cdot |V_{in}|}$$ [Taking magnitude only).

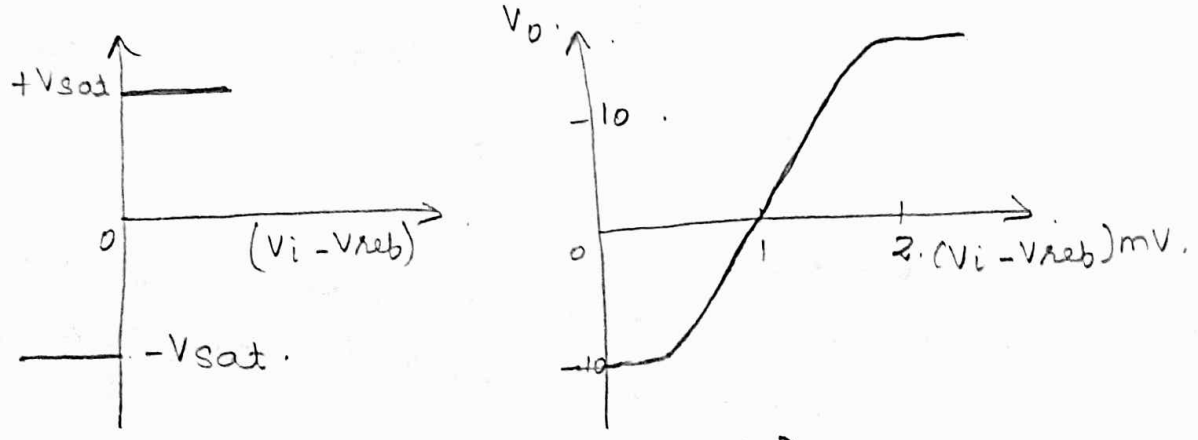
output V_o is proportional to square root of magnitude of V_{in}. V_{in} range between -1 & -10 V.



Finding square roots.

comparators :-

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other output.



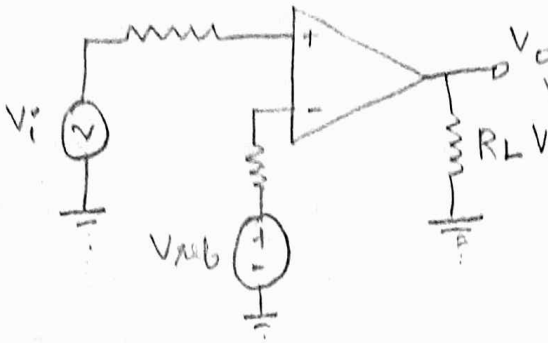
Transfer characteristics (a) Ideal comparator
(b) practical comparator.

Classification of comparators

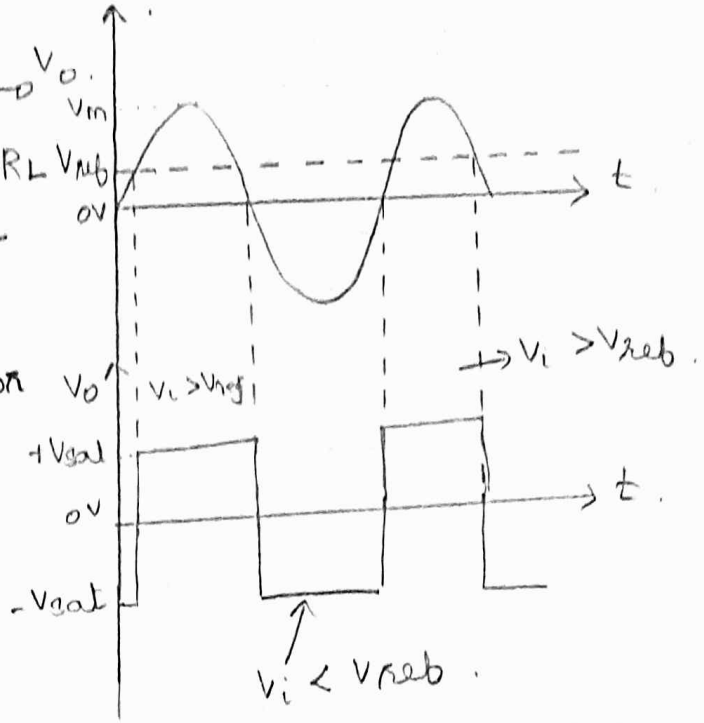
i) Non-inverting comparator.

ii) Inverting comparator.

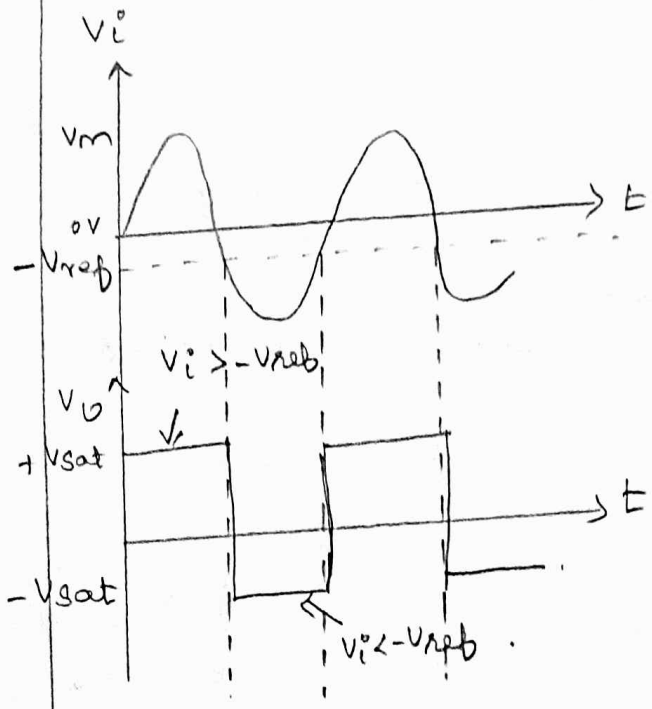
(i) Non-inverting comparator:



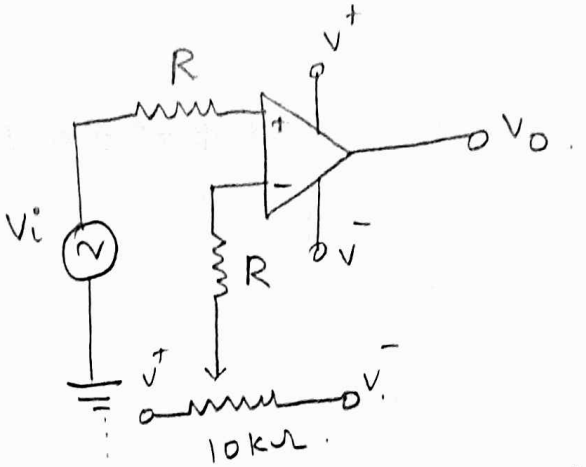
(a) Non inverting comparator



(b) Vref +ve.



(c) Vref Negative



(d) practical Non-inverting comparator.

=> A fixed reference voltage V_{ref} is applied to (-) input and a time varying signal V_i is applied to (+) input.

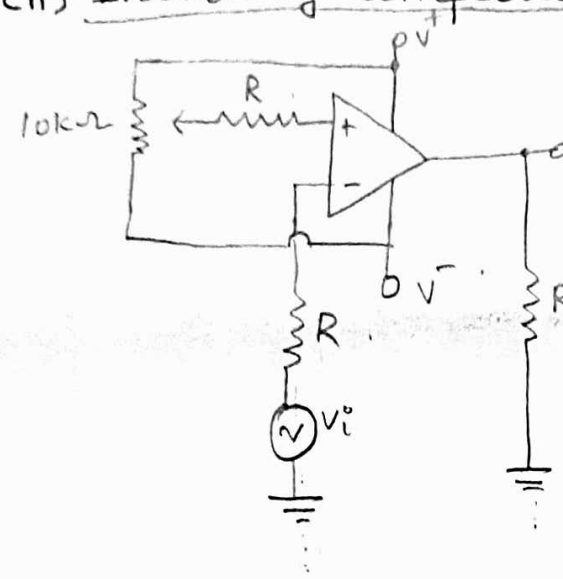
=> The output voltage is at $-V_{sat}$ for $V_i < V_{ref}$.

The output voltage is at $+V_{sat}$ for $V_i > V_{ref}$.

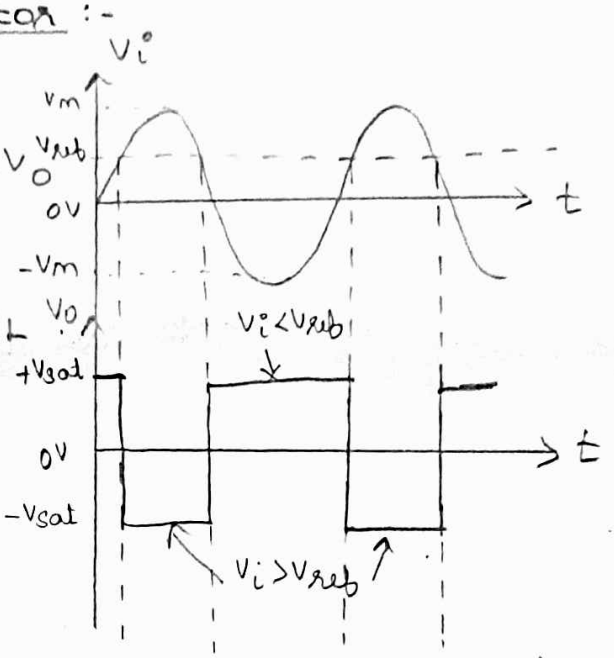
=> The output waveform is a sinusoidal input signal applied to the (+) input.

=> In a practical circuit, V_{ref} is obtained by using a 10kΩ potentiometer which forms a voltage divider with the supply voltages V^+ & V^-. V_{ref} obtained by adjusting the 10kΩ potentiometer.

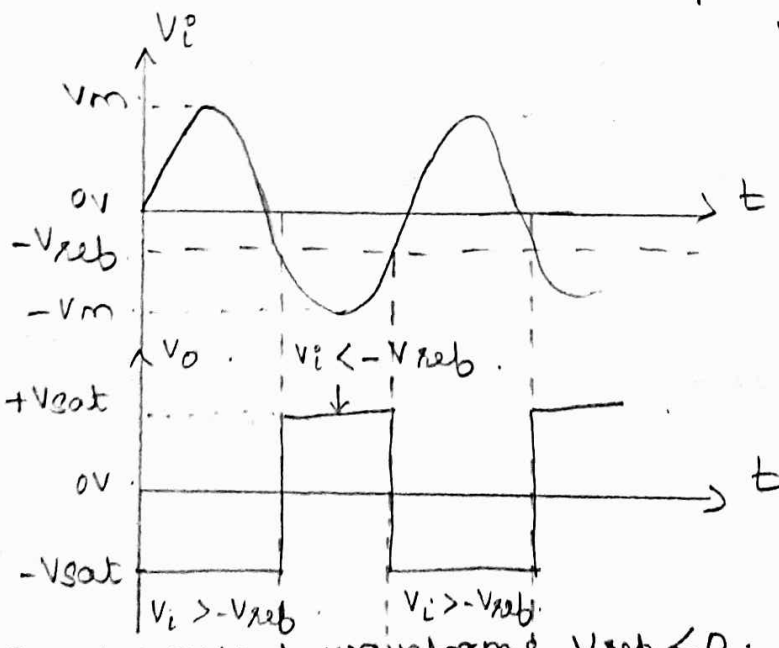
(iii) Inverting comparator :-



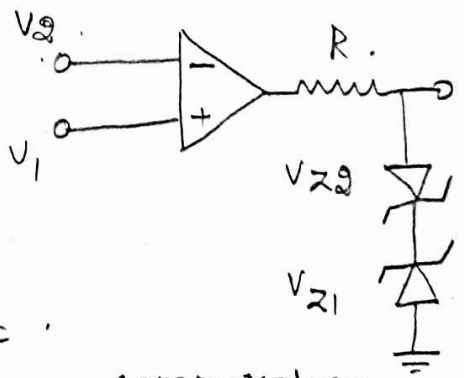
a) Inverting comparator



Input & output waveforms $V_{ref} > 0$.



Input & output waveforms $V_{ref} < 0$.



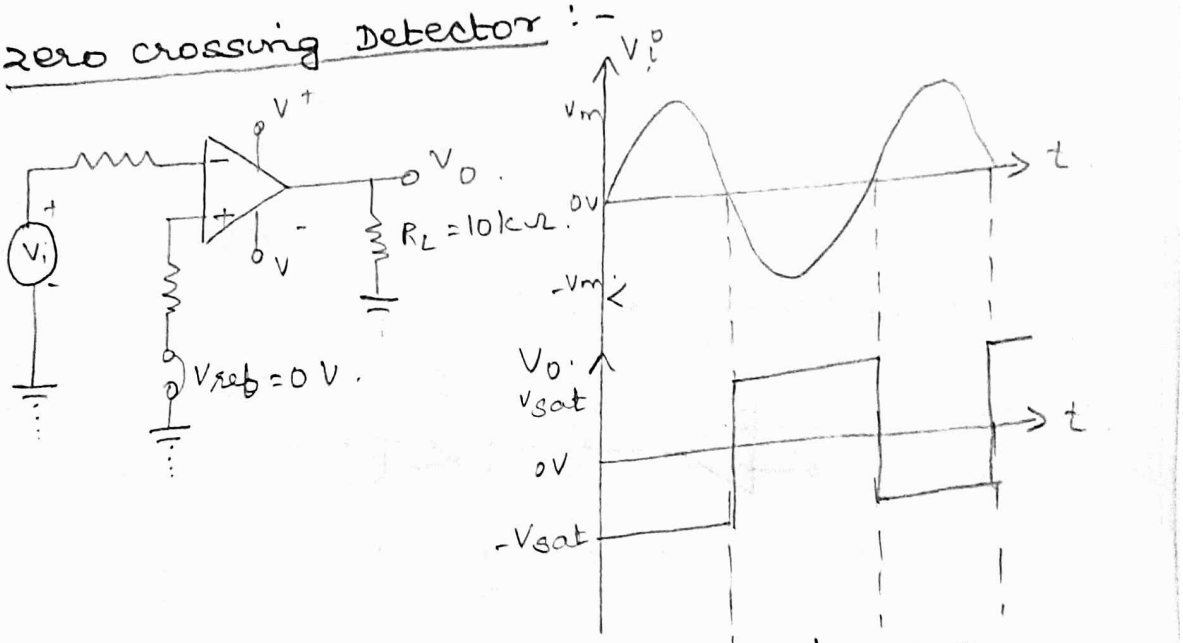
comparator with zener diode at the output.

As a practical Inverting comparator, reference voltage is applied to the (+) input and Vi is applied to (-) input.

Applications of comparator :-

i) Zero crossing Detector.
ii) Window Detector.
iii) Time marker generator.
iv) phase meter.

(i) Zero crossing Detector :-

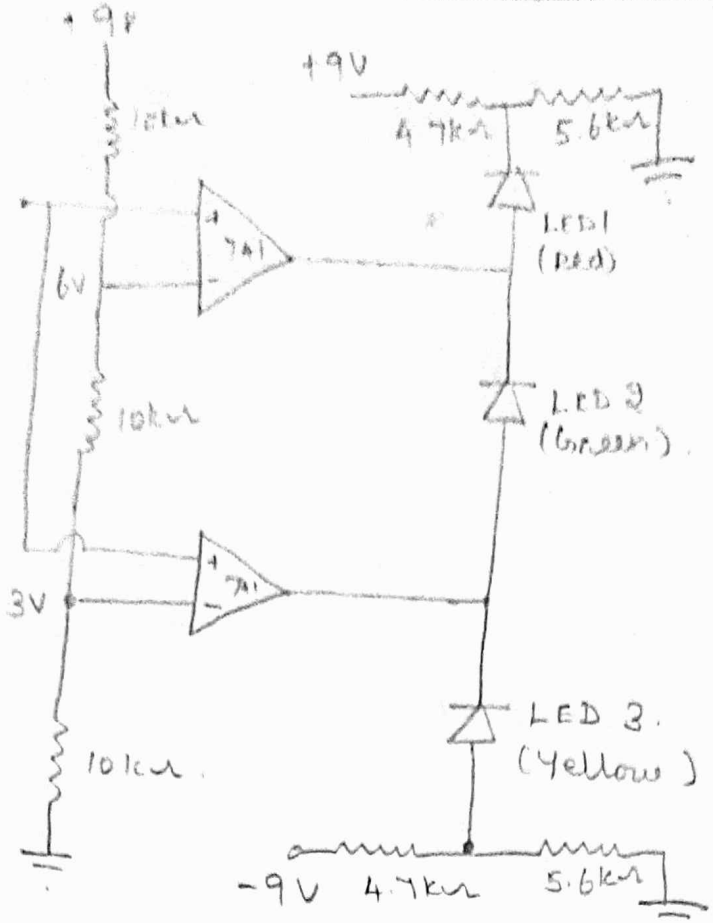


The basic comparator can be used as a zero crossing detector provided that Vref set to zero. The circuit is also called sine to square wave generator.

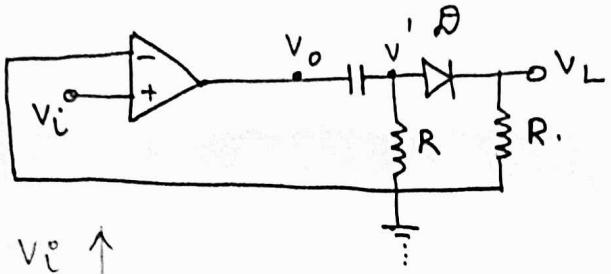
(ii) Window Detector :-

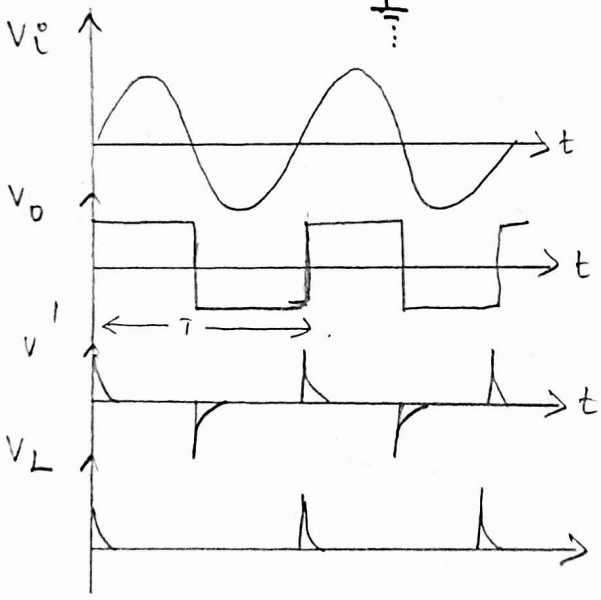
Window Detector circuit is used to mark the instant at which an unknown input is between two threshold levels. 3 indicators are used.

Input (volts)	Yellow LED 3	Green LED 2	Red LED 1.
Less than 3 V	ON	~~obb~~	~~obb~~
Between 3V & 6 V	OFF	ON	~~obb~~
Greater than 6 V	OFF	~~obb~~	on.



Time Marker Generator :-





⇒ The output of the zero-crossing detector is differentiated by an RC circuit ($RC << T$).

⇒ The voltage V' is a series of +ve & -ve pulses.

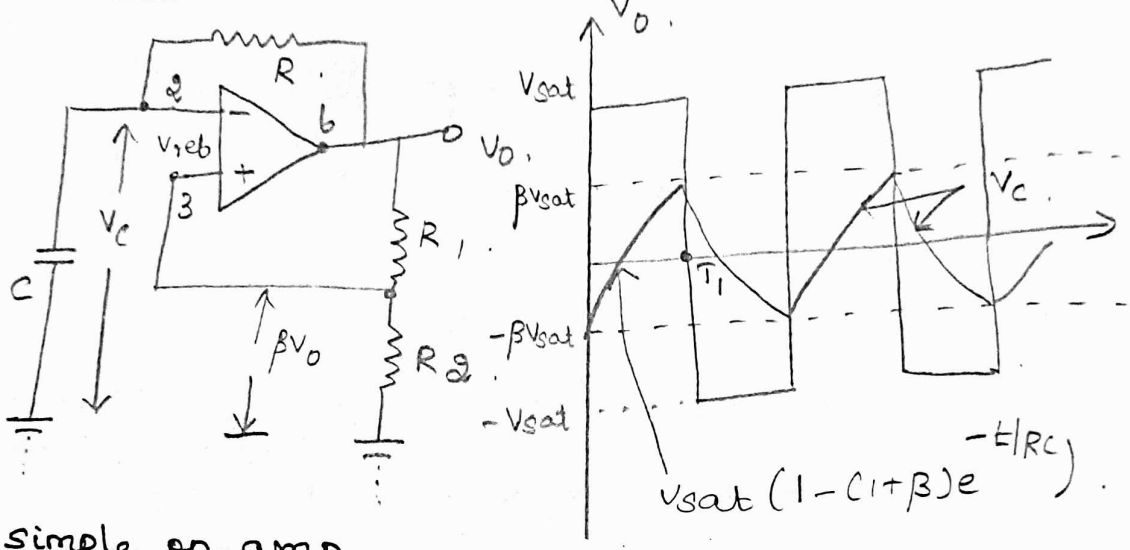
⇒ The negative portion is clipped off after passing

through the diode D and the waveform V_L. The sinusoid has been converted into a train of +ve pulses of spacing T and may be used for triggering the monoshots, SCR, sweep voltage of CRT etc.

Phase Detector :-

phase angle between the voltages can also be measured using the previous circuit. Both voltages are converted into spikes and the time interval between the pulse spikes of one input and that of the other is measured. One can measure phase angles from 0° to 360° with such a circuit.

Square wave Generator (Astable Multivibrator)



simple op-amp square wave generator

waveforms.

=) It is also called free running oscillator.

Fraction $\beta = \frac{R_2}{R_1 + R_2}$ of the output is fed back to the (+) input terminal.

=) Reference voltage V_{reb} is βV_o. It takes $+\beta V_{sat}$ or $-\beta V_{sat}$.

=) The output is fed back to the (-) input terminal after integrating by means of low pass RC combination.

=) At instant of time, when the output is at $+V_{sat}$. the capacitor starts charging towards $+V_{sat}$ through R.

=) The voltage at the (+) input terminal is held at $+\beta V_{sat}$ by R_1 & R_2 combination. This state continues charges on C rises, until it has exceeded $+\beta V_{sat}$, the reference voltage.

=) Voltage at the (-) input terminal becomes greater than this reference voltage, the output is $-V_{sat}$. Voltage on the capacitor is $+\beta V_{sat}$.

=) It begins to discharge through R, charges toward $-V_{sat}$.

Voltage across the capacitor,

$$V_c(t) = V_f + (V_i - V_f)e^{-t/RC}.$$

Final value $V_f = +V_{sat}$.

Initial value $V_i = -\beta V_{sat}$.

$$V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})e^{-t/RC}.$$

$$V_c(t) = V_{sat} - V_{sat}(1+\beta)e^{-t/RC}.$$

At $t = T_1$, voltage across the capacitor reaches βV_{sat} & switching takes place.

$$V_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}(1+\beta)e^{-T_1/RC}.$$

$$T_1 = RC \ln \frac{1+\beta}{1-\beta}.$$

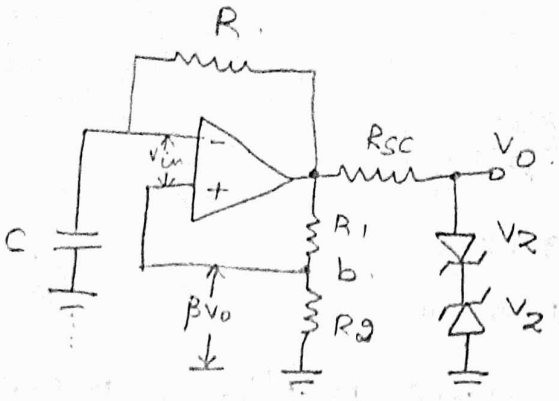
Total time period $T = 2T_1 = 2RC \ln \frac{1+\beta}{1-\beta}$.

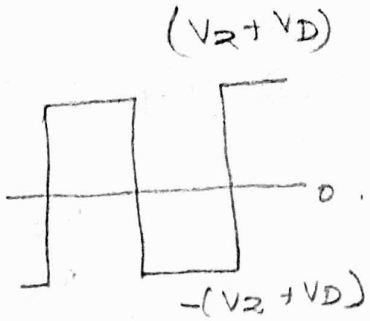
If $R_1 = R_2$, $\beta = 0.5$, $T = 2RC \ln 3$.

$R_1 = 1.16 R_2$. $T = 2RC$. The o/p swings from $+V_{sat}$ to $-V_{sat}$.

$$f_o = \frac{1}{2RC}.$$

V_o peak to peak $= 2V_{sat}$.





use of back to back zener diodes

Peak to peak output amplitude can be varied by varying the power supply voltage. A better technique is to use back to back zener diodes.

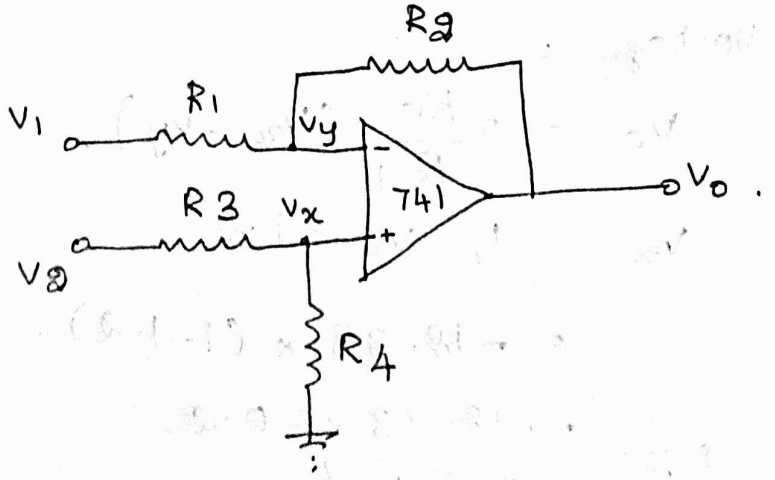
$$V_o(\text{peak to peak}) = 2(V_z + V_D).$$

R_{sc} → limits the current drawn from the op-amp.

$$I_{sc} = \frac{V_{sat} - V_z}{R_{sc}}.$$

Problems :-

① Find the following for the given op-amp differential amplifier : i) The gain of the amplifier ii) The input resistance iii) Output voltage, when the inputs are $1\sin(2000t)$ V & $1.2\sin(2000t)$ V and the $R_1 = R_3 = 1.2k\Omega$, $R_2 = R_4 = 22k\Omega$.



(i) gain $= -\frac{R_F}{R_1}$.

$R_F = 22\,k\Omega$.

$R_1 = 1.2\,k\Omega$.

The gain of inverting amplifier is same as that of differential amplifier.

$$= -\frac{22}{1.2}$$

$$\boxed{\text{Gain} = 18.33}$$

(ii) Input resistance :

With $V_y = 0V$,

Inverting amplifier, input resistance is,

$R_{iFx} = R_1 = 1.2\,k\Omega$.

Similarly $V_x = 0V$,

Non inverting amplifier, input resistance is,

$R_{iFy} = (R_2 + R_3)$.

$= 22 + 1.2\,k\Omega$.

$= 23.2\,k\Omega$.

iii) output voltage :

$$V_o = -\frac{R_F}{R_1}(V_x - V_y).$$

$V_x = 1$, $V_y = 1.2$.

$= -18.33 \times (1 - 1.2)$.

$= -18.33 \times -0.2$

$$\boxed{V_o = 3.666V}$$

UNIT - V

APPLICATION ICs:

AD623 Instrumentation Amplifier and its application as load cell weight measurement - IC voltage regulators - LM78xx, LM79xx, Fixed voltage regulators its application as Linear Power supply - LM317, 723 variability voltage regulators, switching regulators - SMPS - ICL8038 Function generator IC.

LM78xx & LM79xx Three terminal IC voltage regulators:

⇒ 78xx series are 3 terminal, positive, fixed voltage regulators.

⇒ 7 output voltage options available such as 5, 6, 8, 12, 15, 18 & 24V.

⇒ In 78xx the last two numbers xx indicate the output voltage. For e.x 7815 represents a 15V regulators.

⇒ 79xx series are 3 terminal, negative fixed voltage regulators.

⇒ Two extra voltage options of -2V & -5.2V available in 79xx series.

Two packages
i) Metal package (TO-3 type).
ii) Plastic package (TO-220 type).

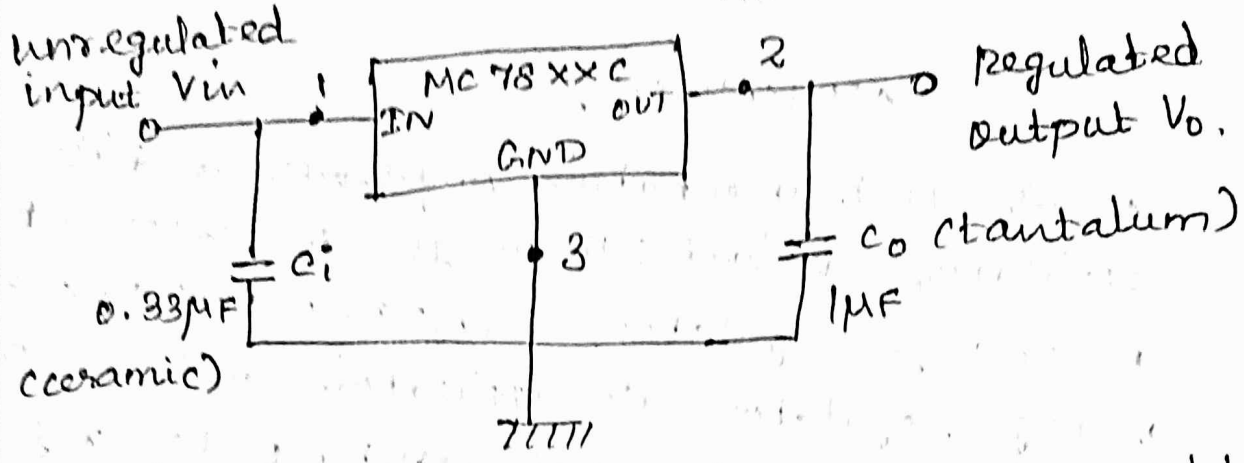


Fig: standard Representation of a +ve regulator.

Device type	output voltage	Device type	Output voltage
7805	5.0V	7905	−5.0V
7806	6.0V	7906	−6.0V
7808	8.0V	7908	−8.0V
7812	12.0V	7912	−12.0V
7815	15.0V	7915	−15.0V
7818	18.0V	7918	−18.0V
7824	24.0V	7924	−24.0V
		7908	−8.0V
		7905.2	−5.2V.

Line/Input Regulation:

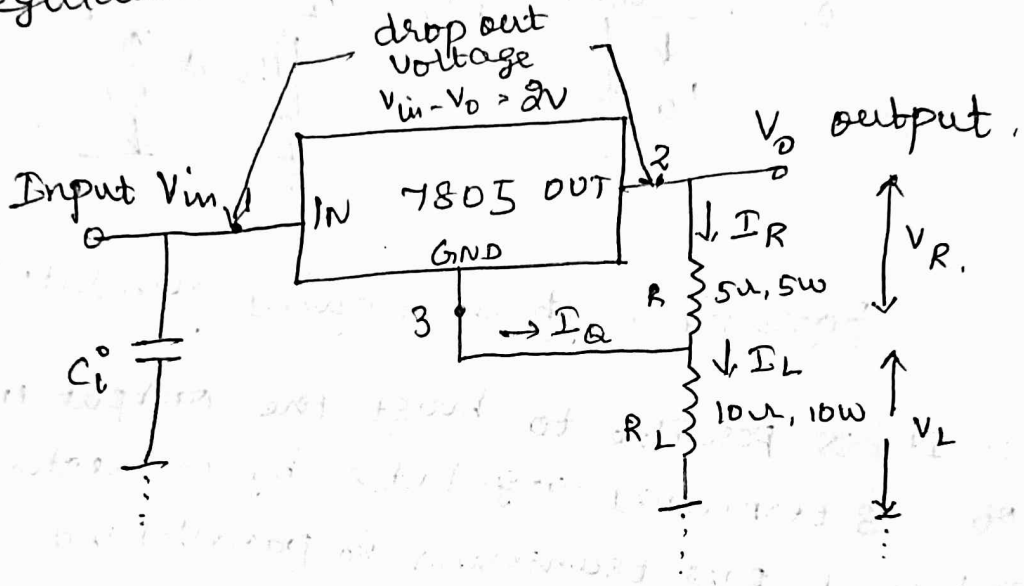
It is defined as the percentage change in the output voltage for a change in the input voltage. It is usually expressed in millivolts or as a percentage of the output voltage. Values are 3 mV.

Load Regulation :-

It is defined as the change in output voltage for a change in load current and is expressed in mV. Values are 15mV for 5mA in 7805 IC.

IC 7805 As a current source :-

The three terminal fixed voltage regulator can be used as a current source.



IC 7805 as a current source.

7805 has been wired to supply a current of 1 ampere to a 10Ω, 10W load.

$$I_L = I_R + I_Q.$$

$I_Q \rightarrow$ quiescent current (4.2mA for 7805)

$$I_L = \frac{V_R}{R} + I_Q.$$

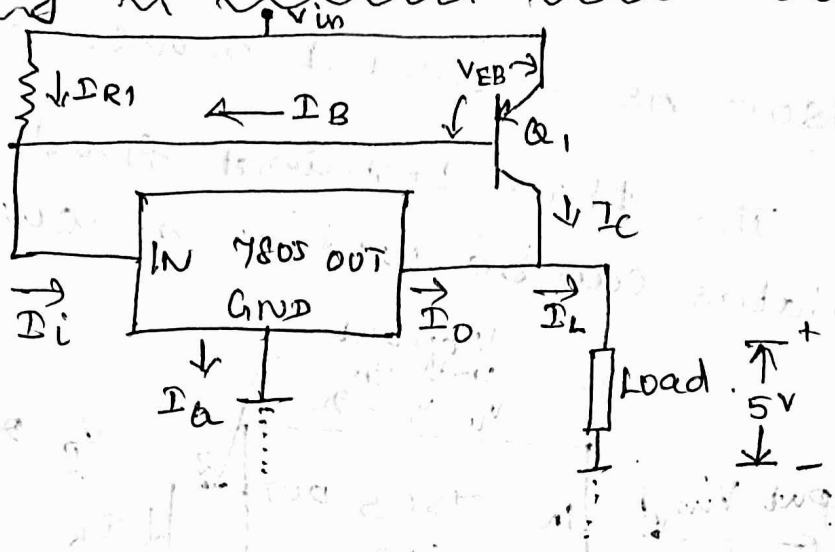
Since $I_L = 1A$, $\frac{V_R}{R} = 1A$ ($I_Q << I_L$).

$$V_R = 5V. \text{ (between terminal 2 \& 3).}$$

$$\therefore R = \frac{V_R}{I_L} = \frac{5V}{1A} = 5\Omega.$$

Thus choose $R = 5\Omega$ to deliver 1A current to a load of 10Ω.

Boosting IC Regulator Output current:



Boosting a three terminal regulator.

⇒ It is possible to boost the output current of a 3 terminal regulator by connecting an external pass transistor in parallel with the regulator.

⇒ For low load current, voltage drop across R, is insufficient (< 0.7 V) to turn on Transistor Q_1, The regulator supply the load current.

⇒ If i_L ↑ voltage drop across R_1 ↑, when voltage drop approximately 0.7 V, Q_1 turns on.

⇒ If i_L = 100 mA, voltage drop across $R_1 = 7\Omega \times 100mA$

= 0.7 V.

$I_L = I_C + I_O$ — (1).

$I_C = \beta I_B$ — (2).

$I_O = I_i - I_Q$.

$I_O = I_i$ (As I_Q is small).

$I_B = I_i - I_{R1}$.

$I_B = I_O - \frac{V_{EB(ON)}}{R_1}$ — (3).

$I_O = I_L - I_C$. (from (1))

$I_O = I_L - \beta I_B$ (from (2)).

(3) $\Rightarrow$ $I_B = I_L - \beta I_B - \frac{V_{EB(ON)}}{R_1}$.

$I_L = I_B + \beta I_B + \frac{V_{EB(ON)}}{R_1}$.

$= (1+\beta) I_B + \frac{V_{EB(ON)}}{R_1}$.

Sub eqn (3) for I_B.

$I_L = (1+\beta)\left[I_O - \frac{V_{EB(ON)}}{R_1}\right] + \frac{V_{EB(ON)}}{R_1}$.

$= I_O - \frac{V_{EB(ON)}}{R_1} + \beta I_O - \beta \frac{V_{EB(ON)}}{R_1} + \frac{V_{EB(ON)}}{R_1}$.

$$\boxed{I_L = (1+\beta) I_O - \beta \frac{V_{EB(ON)}}{R_1}}$$

Applications of IC 78xx & 79xx :-

1) IC 7805 used to provide constant 5V supply to the digital circuits.

2) IC 7812 & 7912 are used to provide dual supply of ±12V to op-amp used in the electronic circuits.

LM317 : Three Terminal Adjustable Regulators:

=) The output voltage can be adjusted from 1.2V to as high as 57V.

=) The common terminal ADJUSTMENT (ADJ) is used for the control of input.

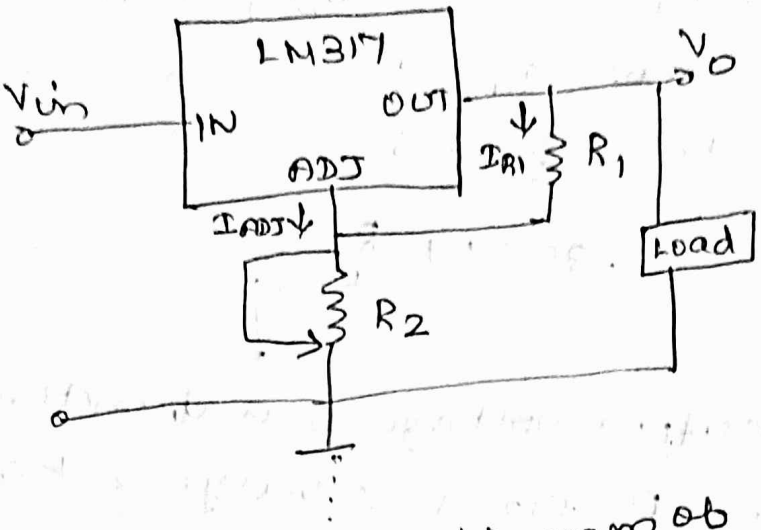
	Type	output voltage	output current
E.x :	LM317	+1.2V to 57V	1.5A
	LM337	−1.2V to −47V	1.5A
	LM358	1.2V to 32V	5A
	LM350	1.2V to 32V	3A
	LM396	1.25 to 15V	10A.

Adjustable voltage regulators has the following advantages :-

1) Improved line & load regulation by a factor of 10 or more.

2) Improved overload protection, greater load current can be drawn

3) Improved reliability for the power supply.



Schematic diagram of LM317.

⇒ LM317 requires only two external resistance R_1 & R_2 to set the required output voltage.

⇒ Internally it develops a reference voltage of 1.25V between OUT & ADJ terminals which is denoted as V_{REF}. This voltage is impressed across the resistance R_1.

⇒ For constant V_{REF} & R_1, the current I_{R1} is also constant. So, R_1 is called current set resistor or program resistor.

By KVL we can write,

$$V_o = V_{R1} + V_{R2}$$

$$V_o = I_{R1} R_1 + (I_{R1} + I_{ADJ}) R_2$$

$$I_{R1} = \frac{V_{REF}}{R_1} = \frac{1.25}{R_1}$$

$$V_o = 1.25 + \frac{1.25}{R_1} \cdot R_2 + I_{ADJ} R_2$$

$$\boxed{V_o = 1.25 \frac{(R_1 + R_2)}{R_1} + I_{ADJ} R_2}$$

The current I_{ADJ} is very small and hence the drop $I_{ADJ}R_2$ is also very small and can be neglected.

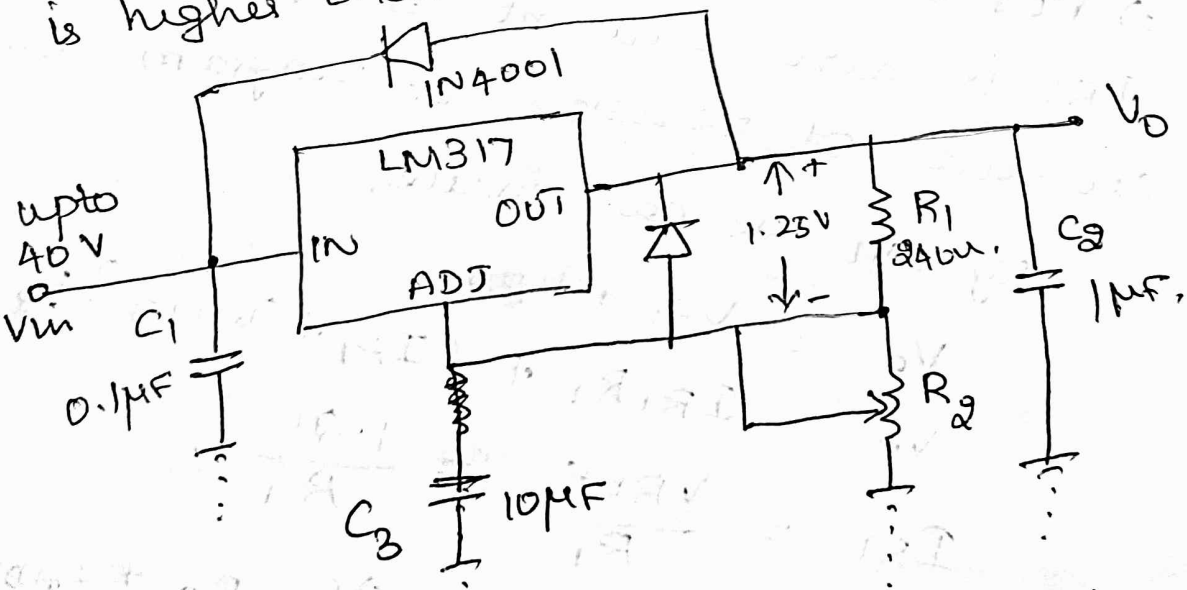
$$V_o = 1.25\left(1 + \frac{R_2}{R_1}\right)$$

The output voltage is a function of R_1 & R_2. By keeping R_1 fixed & varying R_2, the output voltage can be adjusted. The program resistor R_1 is generally 240Ω.

LM317 is located far from the power supply filter then C_1, C_2 are required. C_1 is 0.1 μF disc or 1 μF tantalum.

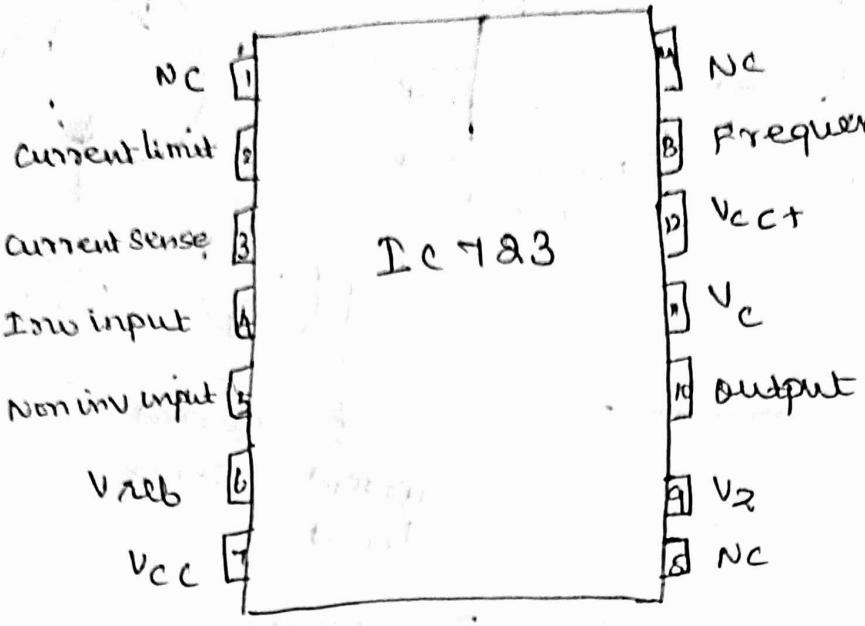
C_2 : 1 to 1000 μF.

Diodes are necessary if output voltage is higher than 25V.



Functional diagram of LM317.

General Purpose Linear IC 723 Regulator :-

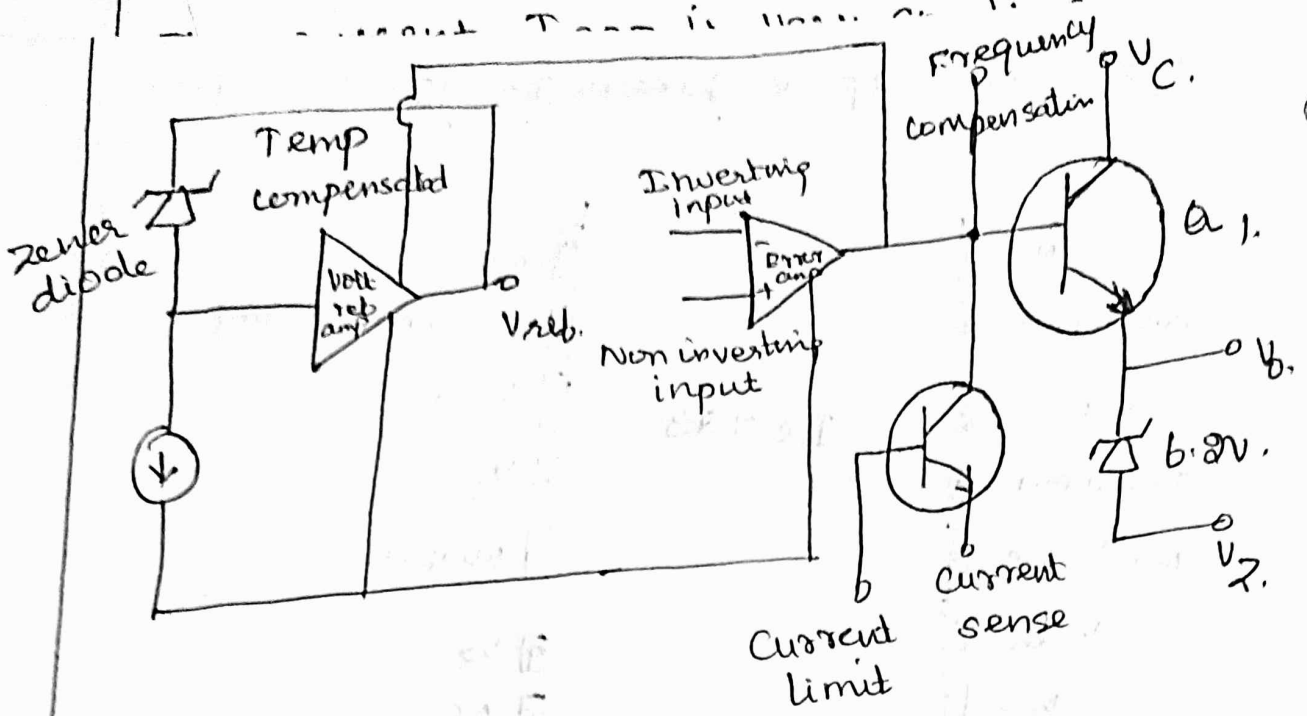


Features of IC 723 :-

1) It works as a voltage regulator at output voltage ranging from 2 to 37 V at currents upto 150mA.
2) used as load currents greater than 150mA
3) I/P & O/P short circuit protection is provided.
4) Good line & Load Regulation (0.03 %).
5) Low temp drift & high ripple rejection.
6) small size, lower cost.
7) provides a choice of supply voltage.

Internal structure of IC 723 :-

1) An op-amp circuit used as an error amplifier.
2) Transistor used to limit output current.



Functional Block Diagram.

=) Output voltage is compared with temp compensated reference potential of the order of 7 Volts. For this Vref is connected to the non-inverting input of the error amplifier.

=) Error amplifier is high gain differential amplifier. It's inverting input is connected to the either whole regulated output voltage or part of that from outside.

=) Error amplifier controls the series pass transistor Q_1, which acts as variable resistor. The unregulated power supply source is connected to collector of series pass transistor.

=) Q_2 acts as current limiter.

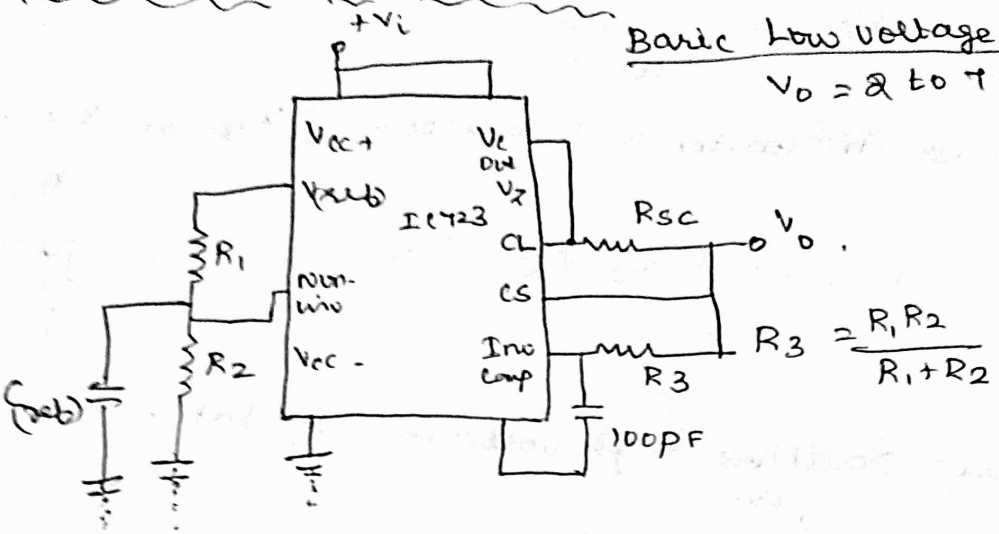
=) Frequency compensation terminal controls

the frequency response of the error amplifier.

Applications of IC 723 :-

(1) Basic Low Voltage Regulator.

V_o = 2 to 7 volts.



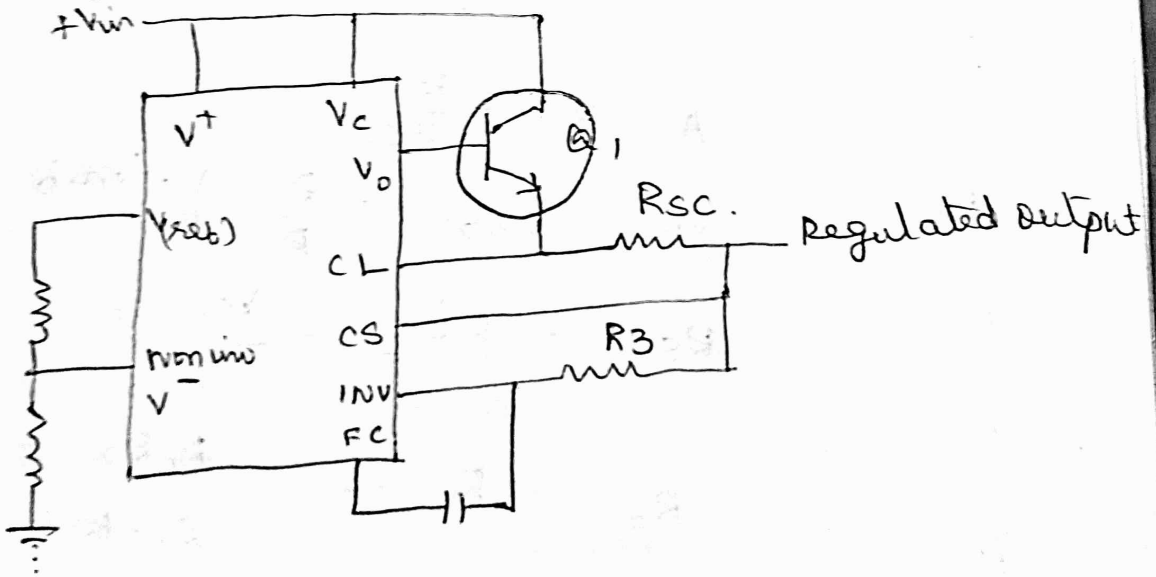
$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

$$R_{sc} = \frac{V_{sense}}{I_{limit}} = \frac{0.6}{I_{limit}}$$

$$V_{non\text{-}inverting} = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

$$V_o = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

(2) Low voltage High current regulator :-



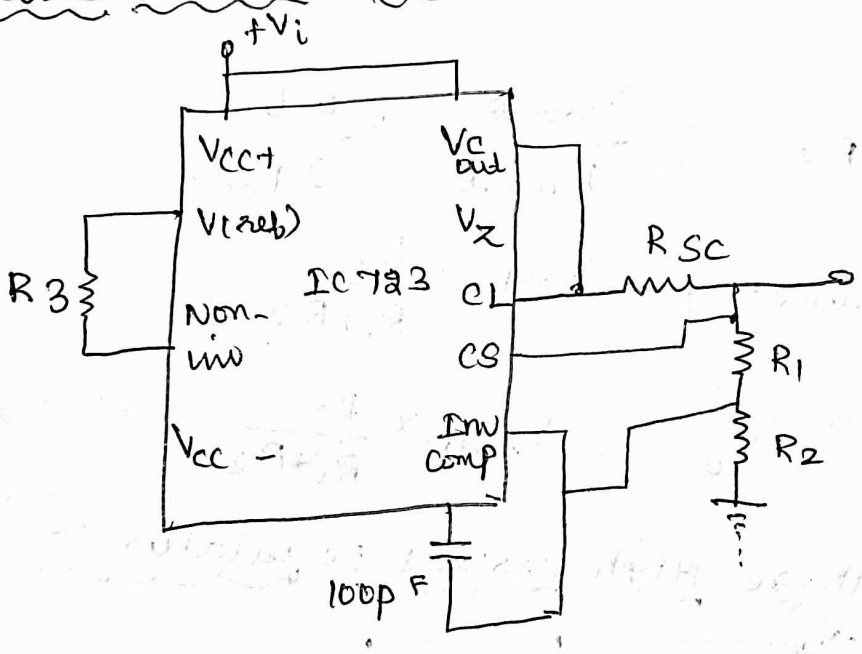
$$V_o = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

$$R_{sc} = \frac{0.6}{I_{limit}}$$

Power dissipation of Transistor $= [V_{icmax} - V_{ocmin}] \times I_{L(max)}$

Power dissipation of $I_C = [V_{icmax} - V_{ocmin}] \times \frac{I_{L(max)}}{h_{fe(min)\,of\,Q}}$

(3) Basic positive high voltage Regulator :-



$$A = 1 + \frac{R_1}{R_2}$$

$$V_o = V_{ref}\left(1 + \frac{R_1}{R_2}\right) = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right)$$

$$R_{sc} = \frac{0.6}{I_{limit}} = \frac{V_{sense}}{I_{sc}}$$

$$R_3 = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Switching Regulators.

⇒ The pulse width modulation is the basic principle of the switching regulators.

⇒ Duty cycle $\delta = \frac{t_{on}}{t_{on} + t_{off}}$

$$\delta = \frac{t_{on}}{T} = t_{on} \times f$$

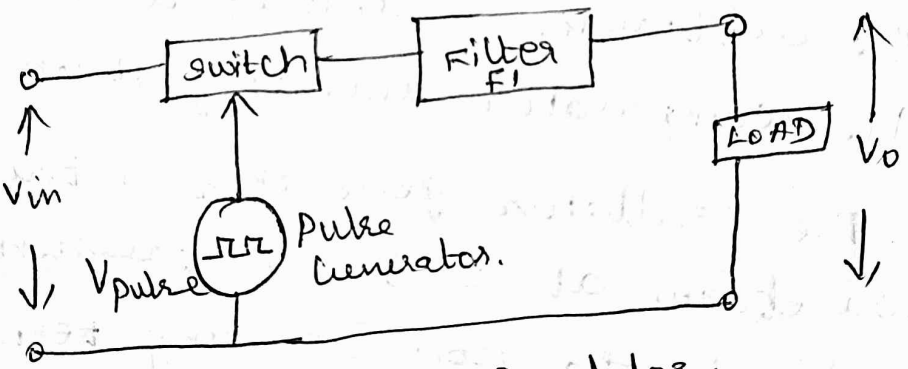
t_{on} → on time of pulse.

t_{off} → off time of pulse.

T → Time period $= t_{on} + t_{off} = \frac{1}{f}$.

Four major components

1) voltage source Vin
2) switching Transistor.
3) Pulse Generator, Vpulse.
4) Filter F_1.

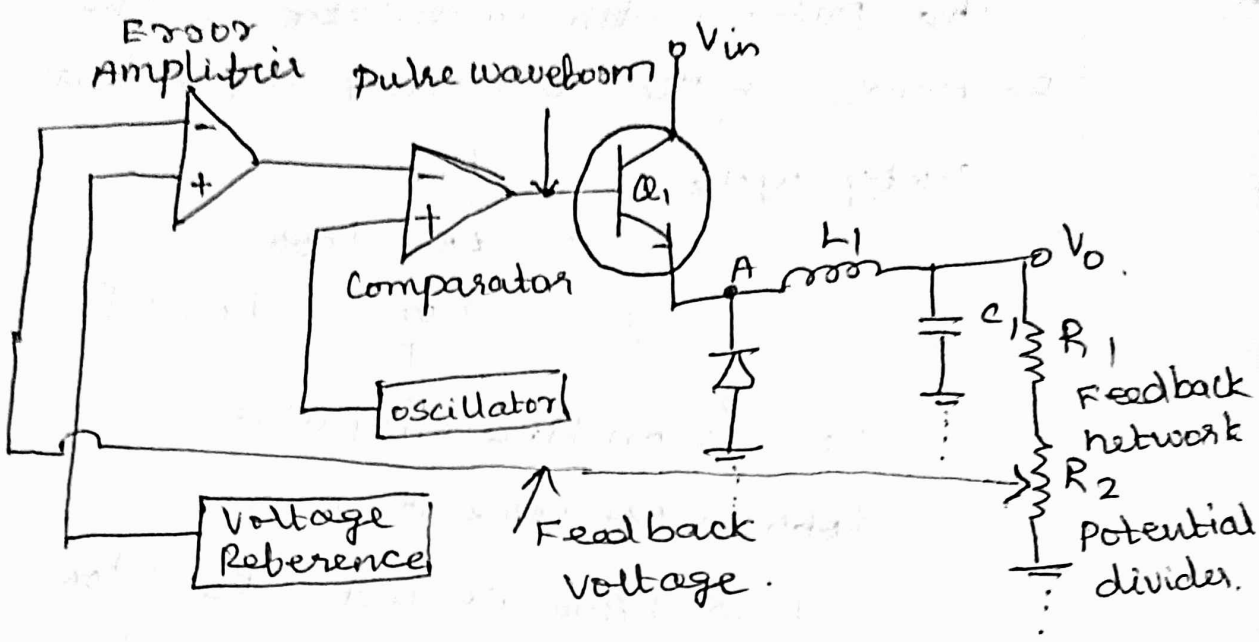


Basic switching Regulator;

⇒ The switch is generally a Transistor. The pulse generator output makes it on & off. Pulse generator produces a required pulse waveform. Frequency range : 20KHz. Operating frequency 10 to 50KHz.

Filter F_1 may be RL, RC, RLC.

Block diagram of SMPS :-



Functional Block diagram of switching Regulator.

⇒ The part $\frac{R_2}{R_1+R_2}$ of the output is fedback to the inverting input of error amplifier. It is compared with the reference voltage. The difference is amplified and given to the comparator inverting terminal.

⇒ The oscillator generates a triangular waveform at a fixed frequency. It is applied to the non-inverting terminal of the comparator.

⇒ Output of comparator is high when the triangular voltage waveform is above the level of the error amplifier output. The duty cycle is controlled by the difference between the feedback voltage & V_{ref}.

$$V_o = \frac{t_{on}}{T} V_{in} = \delta V_{in}$$

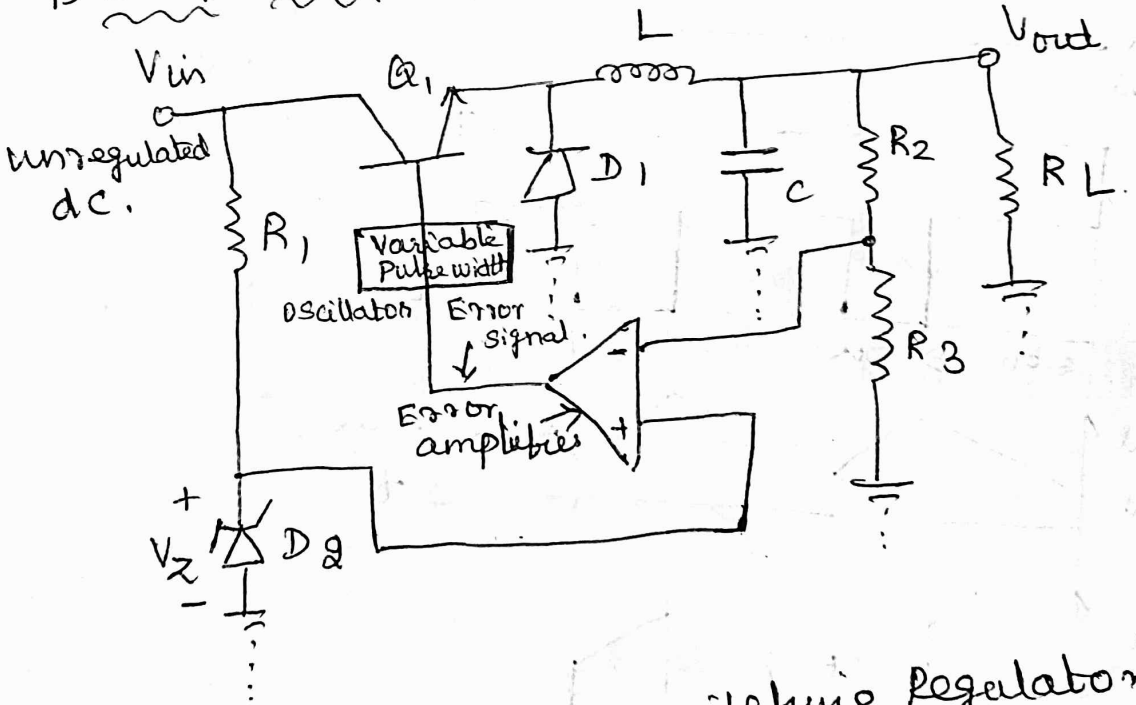
=) when T is constant, output is proportional to ton. This method is called Pulse width Modulation (PWM).

=) when ton is constant, the output is inversely proportional to the period T (f).

Types of switching Regulators :-

1) Buck switching Regulators. (or) step down
2) Boost switching Regulators (or) step up
3) Inverting type switching Regulator.

1) step down (or) Buck Regulators :-



step down switching Regulator.

Operation :-

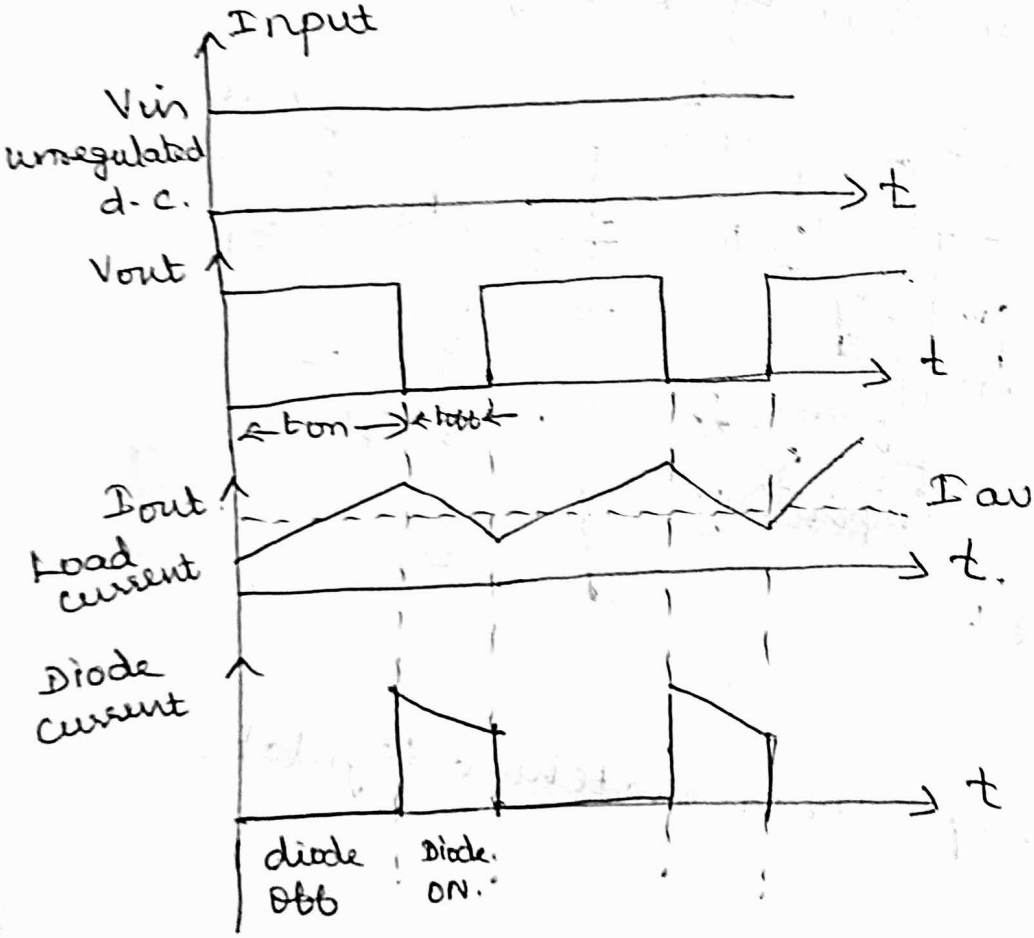
When Q_1 is ON, the capacitor charges through it and Q_1 is OFF, the capacitor discharges through the load Resistance.

The variable pulse width oscillator controls ON/OFF periods of Q_1.

When ON time is more compared to OFF time, capacitor charges more increasing the V_o.

When OFF time is more than ON time for Q_1, capacitor discharges more, reducing V_o.

⇒ Adjust the duty cycle $\delta = \frac{t_{on}}{T}$ of Q_1, output voltage can be regulated.

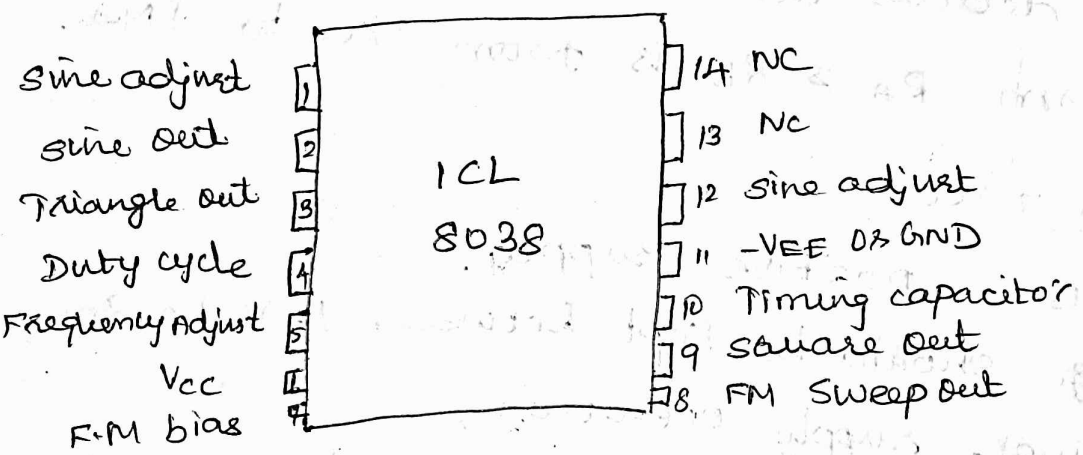


Function Generator ICL 8038 :

Function Generators are designed to provide the basic waveforms such as square wave, triangular wave & sine wave. They are also called as waveform generators.

In function Generators, VCO (voltage controlled oscillator) generates the triangular and square waves.

Pin diagram :-



Pin 1 & Pin 12 : Sine wave Adjust

The external resistor connections to these pins decides the accuracy of the sine wave.

Pin 2 : Sine wave out

The sine wave output is available at this pin. The amplitude of sine wave is 0.22Vcc,

$\pm 5V \leq V_{cc} \leq \pm 15V$.

Pin 3 Triangular wave output:

The triangular wave output is available at this pin. Amplitude of triangular wave is also function of input voltage V_{CC}. It is 0.33 V_{CC}.

Pin 4 & 5 : Duty cycle / Frequency Adjust:

The external resistor R_A & R_B are connected to pin 4 & 5 respectively. The values of R_A, R_B & external capacitor connected at Pin 10 decides the frequency of the output waveform. R_A & R_B is from 1kΩ to 1MΩ.

Pin 6 : +Vcc

It is a positive supply. voltage should be kept between 10 V to 30V, for single supply operation,

$\pm$5V to $\pm$15V → dual supply operation.

Pin 7 : FM bias

Pin 7 is a function of two resistors (R_1 = 10kΩ, R_2 = 40kΩ) that form a potential divider with a supply voltage V_{CC}.

Pin 8 : FM sweep input:

Voltage between V_{CC} & pin 8 decides the output frequency. The output frequency can be controlled by applying external voltage

usually referred to as sweep voltage to pin 8. Sweep voltage is kept between $\left(\frac{2}{3}V_{CC} + 2\right)$ & V_{CC}.

Pin 9 : Square wave output :

Square wave output is available at this pin. External resistor is required to be connected between V_{CC} & pin 9 to get the square wave at pin 9.

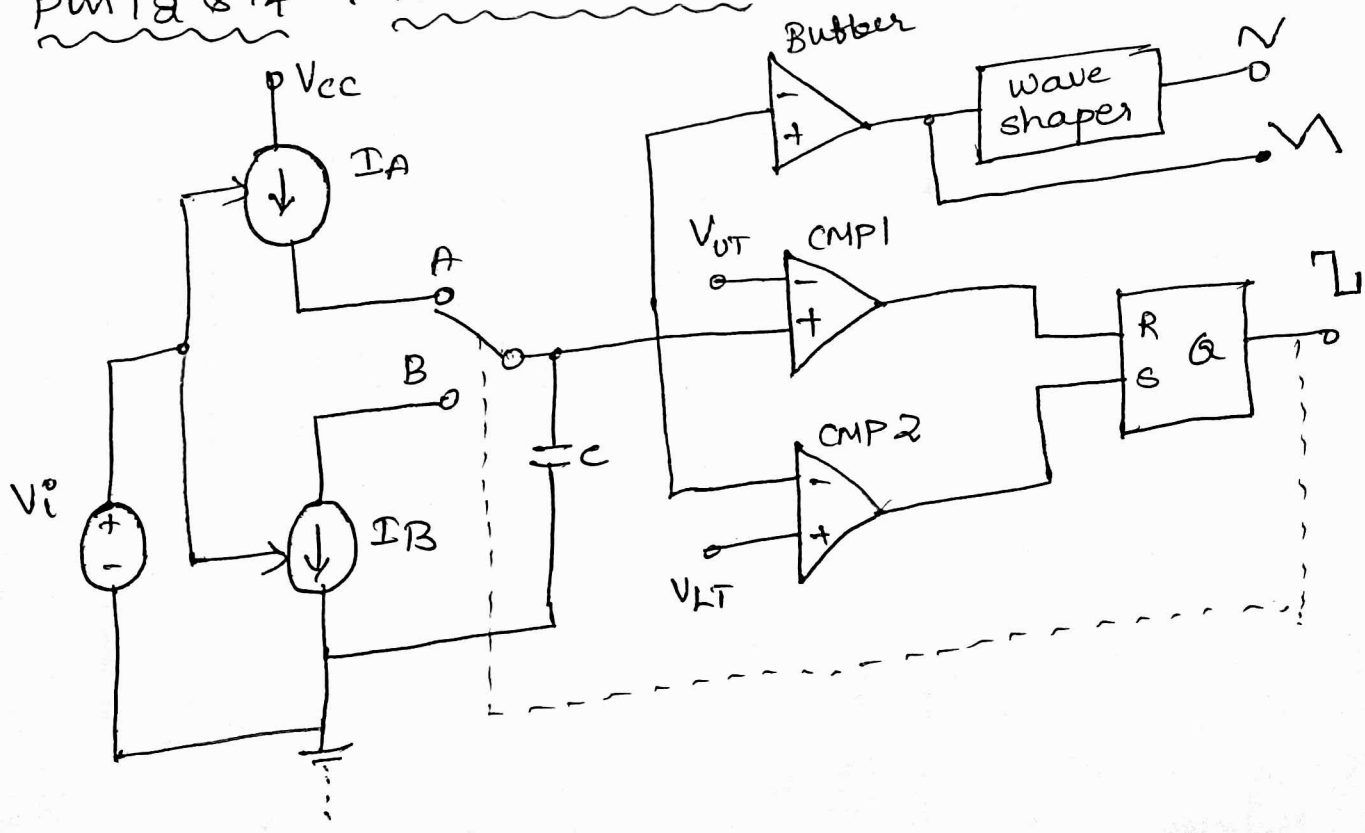
Pin 10 : Timing capacitor

External timing capacitor C is connected at this pin.

Pin 11 : $-V_{EE}$ / Ground

If dual supply is used V_{EE} is connected to this pin. If a single is used, this pin is connected to the ground.

Pin 12 & 14 : Not connected.



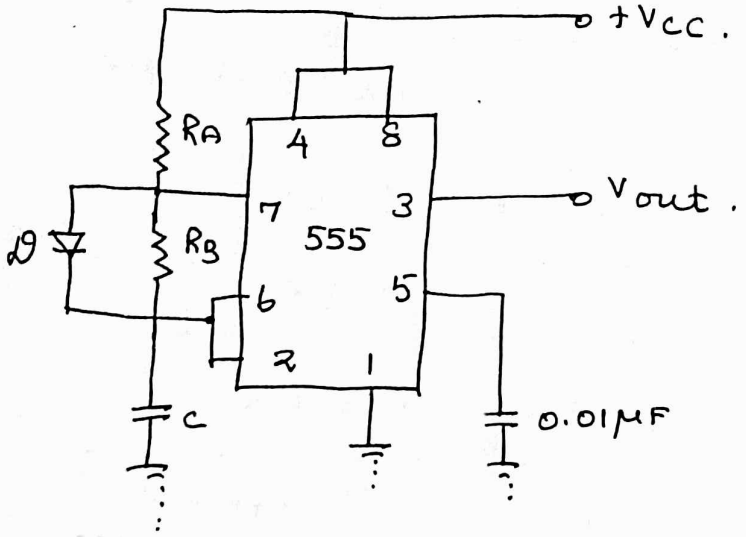
⇒ When switch is at position A, the capacitor charges at a rate determined by current source I_A.

⇒ Once the capacitor voltage reaches V_{UT}, the upper comparator (CMP1) triggers and resets the flip-flop output. This causes the switch position to change from position A to B. capacitor starts discharging at the rate determined by the current sink I_B.

⇒ Once the capacitor reaches V_{LT}, the lower comparator (CMP2) triggers and sets the flip-flop output. This causes the switch position to change from position B to A. This cycle repeats.

④ Design and draw the waveform of a 1KHz square wave generator using 555 timer for duty cycle of 50%.

Step① : Draw the circuit diagram of Astable Multivibrator (Square wave Generator).



Step② calculate the total time period.

$D = 50\%$, $f = 1KHz$.

$$T = \frac{1}{f} = \frac{1}{1\times10^{3}} = 1\times10^{-3} = 1ms.$$

$$D = \frac{T_{ON}}{T}$$

$$T_{ON} = D \times T.$$

$$= 0.5T = 0.5\times1 = 0.5ms.$$

$$T = T_{ON} + T_{OFF}.$$

$$T_{OFF} = T - T_{ON}.$$

$$= 1 - 0.5 = 0.5ms.$$

Choose $C = 0.1\mu F$.

$T_d = 0.69 R_A C$.

For duty cycle 50%. charging time T_c & Discharging time T_d are equal.

$T_d = T_c = 0.5 ms$.

Q.B $\boxed{T_d = 0.69 R_A C}$.

$0.5 = 0.69 \times R_A \times 0.1 \mu F$.

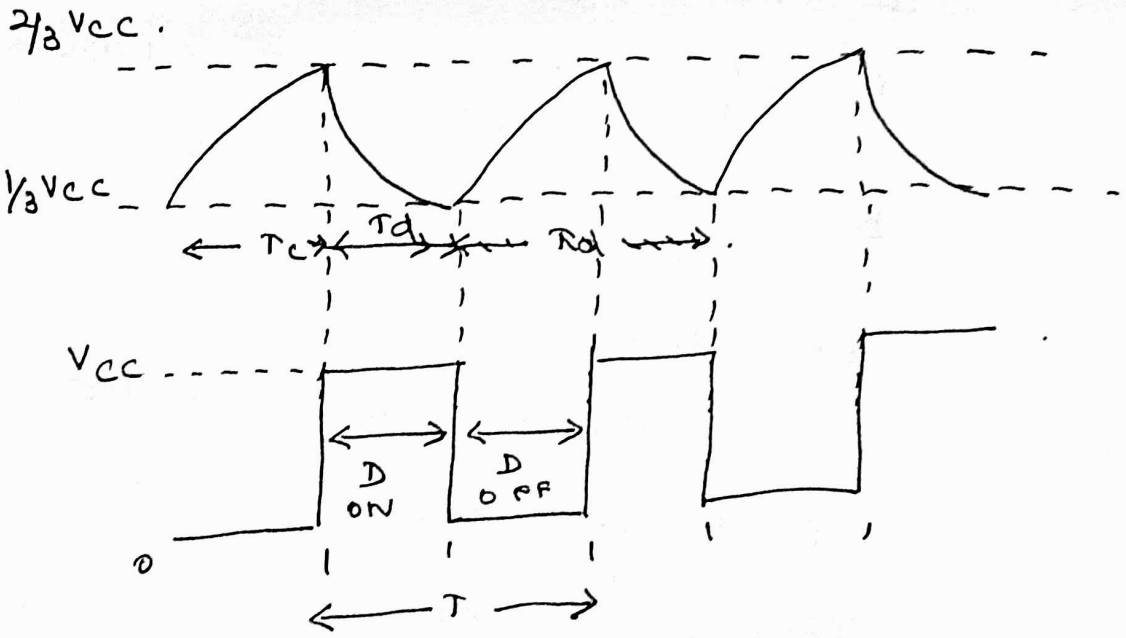
$R_A = 7.246 k\Omega$.

$\boxed{T_c = 0.69 R_B C}$.

$T_c \times R_B = 0.69 \times C$.

$\boxed{R_B = 7.246 k\Omega}$.

waveform:-



$T_c = T_d$, Y.D = 50 Y..

Monostable Multivibrator

- A monostable multivibrator has one stable state and the other is quasi stable state.
- The circuit is useful for generating single output pulse of adjustable time duration in response to the triggering signal.

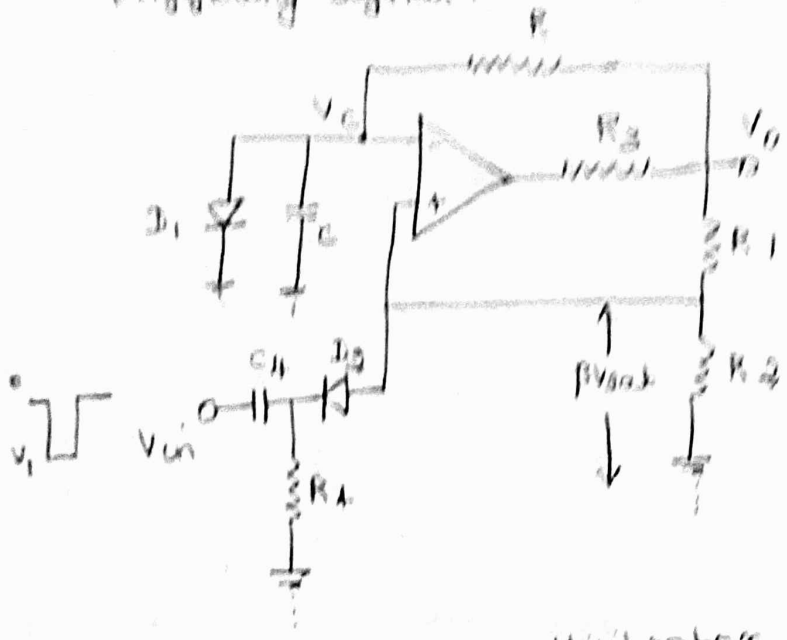
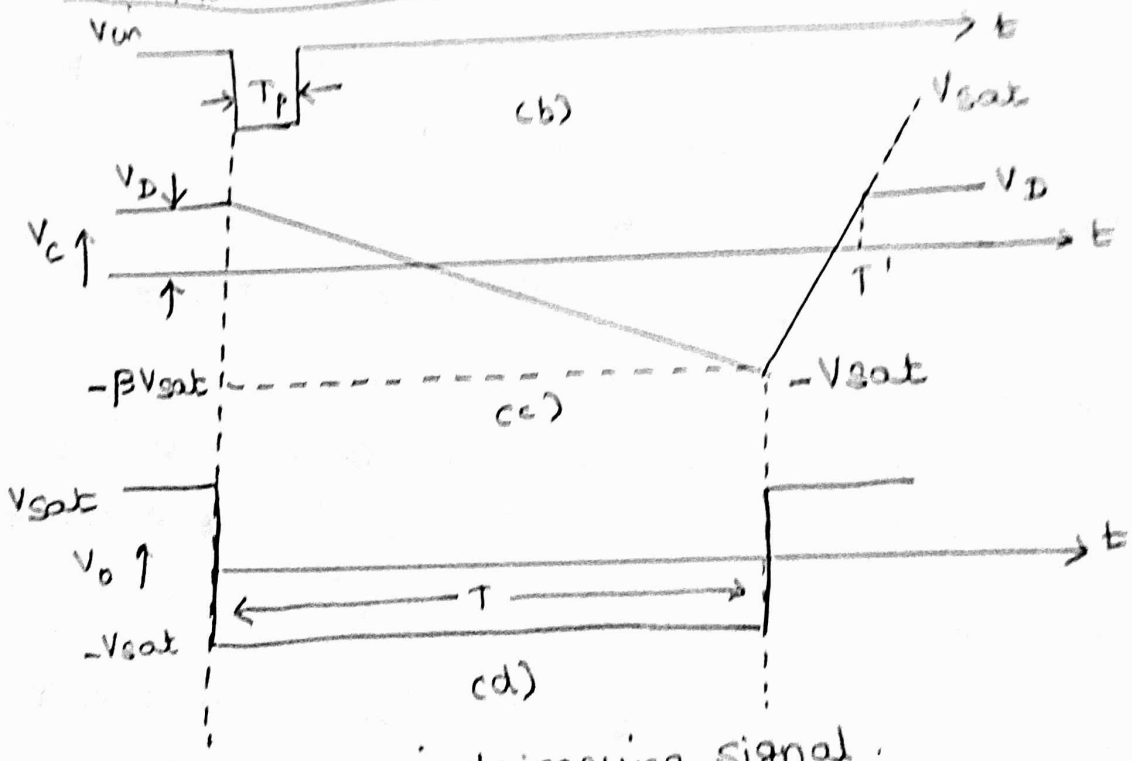


Fig: Monostable multivibrator



(b) → Negative going triggering signal.
(c) → capacitor waveform
(d) → Output voltage waveform.

* It is a modified form of the astable multivibrator.
* Diode D_1 clamps the capacitor voltage to 0.7V, when the output is at $+V_{sat}$.
* A negative going pulse signal of magnitude V_1 passing through the differentiator R_4C_4 and Diode D_2 produces a negative going triggering impulse and applied to the (+) input terminal.

* Circuit Analysis :-

Output V_o is at $+V_{sat}$.

=> Diode D_1 conducts, V_c gets clamped to 0.7V.

=> The voltage at (+) terminal is $+\beta V_{sat}$.

=> A negative trigger of magnitude V_1 is applied to the (+) input terminal, Effective signal $[\beta V_{sat} + (-V_1)] < 0.7V$ op-amp output switch from $+V_{sat}$ to $-V_{sat}$.

=> The diode reverse biased, capacitor charging to $-V_{sat}$.

=> The voltage at the (+) input terminal is $-\beta V_{sat}$.

=> capacitor voltage V_c more than $-\beta V_{sat}$, output of op-amp is $+V_{sat}$.

=> capacitor C starts charging to $+V_{sat}$.

Pulse width T is calculated.

General solution for a single time constant low Pass RC circuit with V_i, V_f as initial & final value is,

$$V_o = V_f + (V_i - V_f)e^{-t/RC}.$$

$V_f = -V_{sat}$, $V_i = V_D$ (diode forward voltage)

$$V_{oc} = -V_{sat} + (V_D + V_{sat})e^{-t/RC}.$$

at $t = T$, $V_c = -\beta V_{sat}$.

$$-\beta V_{sat} = -V_{sat} + (V_D + V_{sat})e^{-T/RC}$$

After simplification,

$$T = RC \ln \frac{(1 + V_D/V_{sat})}{1 - \beta}$$

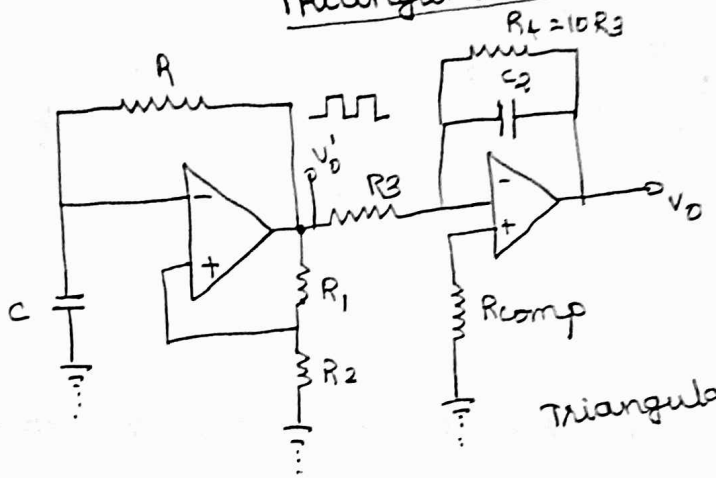
$$\beta = \frac{R_2}{R_1 + R_2}$$

If $V_{sat} >> V_D$, $R_1 = R_2$, $\beta = 0.5$

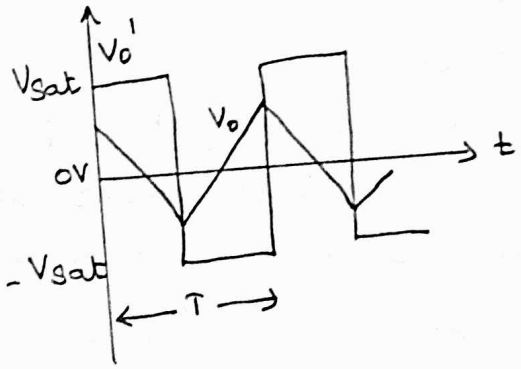
$$\boxed{T = 0.69RC}$$

For monostable operation, the trigger pulse width T_p should be much less than T. (pulse width of monostable Multivibrator).

Triangular Wave Generator



Triangular waveform Generator



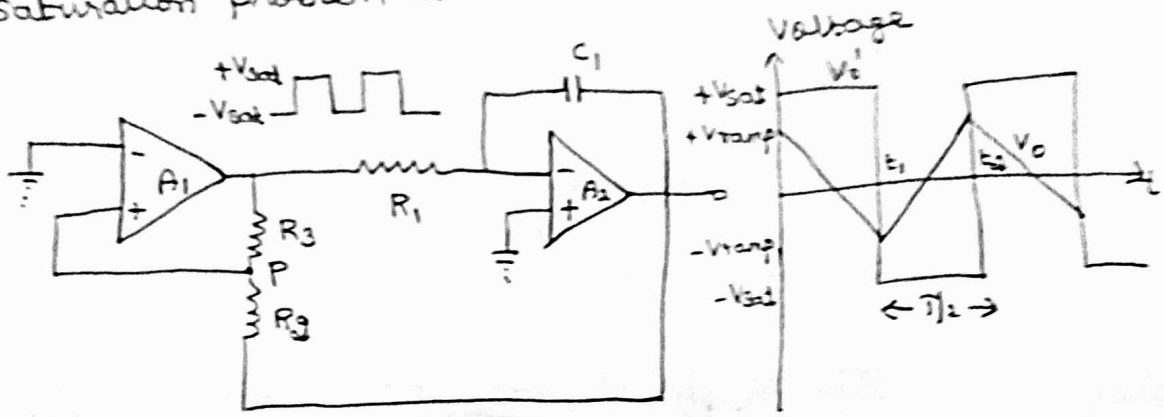
output waveform.

=) A triangular wave can be simply obtained by integrating a square wave.

=) The frequency of the square wave & triangular wave is the same value.

=) Amplitude of square wave is constant at ±Vsat amplitude of triangular wave decrease as the frequency increases, due to reactance of the capacitor C_2 in the feed back circuit.

=) Resistance R_4 connected across C_2 to avoid saturation problem at low frequencies.



(a) Triangular waveform generator using lesser components (b) waveforms.

=) It consists of a two level comparator followed by an integrator. The output of the comparator A_1 is a square wave of amplitude ±Vsat, applied to the (-) input terminal of the integrator A_2 producing a triangular wave. This triangular wave is fed back as input to the comparator A_1 through voltage divider R_2R_3.

=) Let output of Comparator A_1 is at $+V_{sat}$.
output of integrator A_2 negative going ramp. (fig)
one end of the voltage divider $R_2 R_3$ is at $+V_{sat}$
and the other at -ve going ramp of A_2.

=) At a time $t = t_1$, (-ve) going ramp attains a value of $-V_{ramp}$. voltage at point P less than 0V, so output of A_1 switches from +ve saturation to negative saturation level $-V_{sat}$.

=) When the output of A_1 is at $-V_{sat}$, output of A_2 increases in the positive direction.

=) at $t = t_2$, voltage at point P becomes above 0V, swithing the output A_1 from $-V_{sat}$ to $+V_{sat}$.
The cycle repeats & generates a triangular waveform.

=) Amplitude of the triangular wave depends upon the RC value of the integrator A_2 & output voltage level of A1.

Calculation of Triangular waveform frequency:-

=) The effective voltage at point P, when output of A_1 is at $+V_{sat}$ level is given by,

$$-V_{ramp} + \frac{R_2}{R_2+R_3}\left[+V_{sat} - (-V_{ramp})\right].$$

at $t = t_1$, voltage at point P equal to zero.

$$\therefore -V_{ramp} = -\frac{R_2}{R_2+R_3}(+V_{sat})$$

IIIly at $t = t_2$, output of A_1 switches from $-V_{sat}$ to $+V_{sat}$,

$$V_{ramp} = -\frac{R_2}{R_3}(-V_{sat}) = \frac{R_2}{R_3}(V_{sat}).$$

$$-V_{ramp} + \frac{R_2}{R_2+R_3}(+V_{sat} + V_{ramp}) = 0.$$

$$\frac{-V_{ramp}R_2 - V_{ramp}R_3 + R_2 V_{ramp}}{R_2+R_3} = -\frac{R_2}{R_2+R_3}V_{sat} \Rightarrow \boxed{-V_{ramp} = -\frac{R_2}{R_3}(+V_{sat})}$$

peak to peak amplitude, of the triangular wave is,

$$V_{o(PP)} = +V_{ramp} - (-V_{ramp}) = 2\frac{R_2}{R_3} V_{sat} \quad \text{---(1)}.$$

output switches from $-V_{ramp}$ to $+V_{ramp}$ in half the time period $T/2$.

Putting in Integrator equations:

$V_{o(PP)} = +V_{ramp} - (-V_{ramp})$

$= 2\frac{R_2}{R_3} V_{sat}$

$$V_o = -\frac{1}{RC}\int V_i \cdot dt.$$

$$V_{o(PP)} = -\frac{1}{R_1 C_1}\int_0^{T/2} (-V_{sat})\, dt$$

$$= \frac{V_{sat}}{R_1 C_1}\left(T/2\right).$$

$$T = 2R_1 C_1 \frac{V_{d(PP)}}{V_{sat}}$$

from eqn (1), we get

$$T = \frac{4R_1 C_1 R_2}{R_3}$$

Frequency of oscillations is,

$$\boxed{f_o = 1/T = \frac{R_3}{4R_1 C_1 R_2}}$$

clipper circuits.

The circuits which are used to clip off the unwanted portions of the input voltage above or below certain levels, to produce required output are called limiting circuits. These circuits are known as clipping circuits.

classifications :

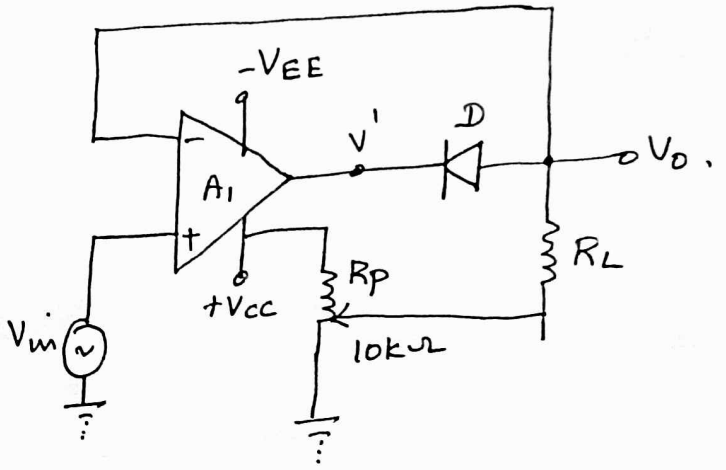
i) Positive clipper circuit

ii) Negative clipper circuit.

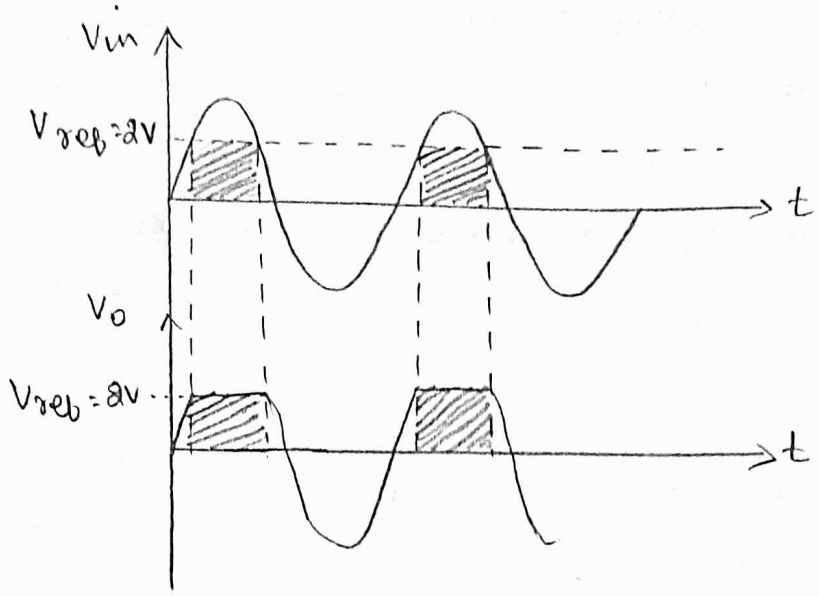
Positive clipper circuit :

The positive clipper circuit remove some positive part from the input to produce the output. The clipping level is determined by the reference voltage Vref.

The reference voltage Vref is obtained from the positive supply voltage +Vcc or negative supply voltage -VEE.



Positive clipper circuit.



waveforms of (+ve) clipper ~~circuit~~ circuit.

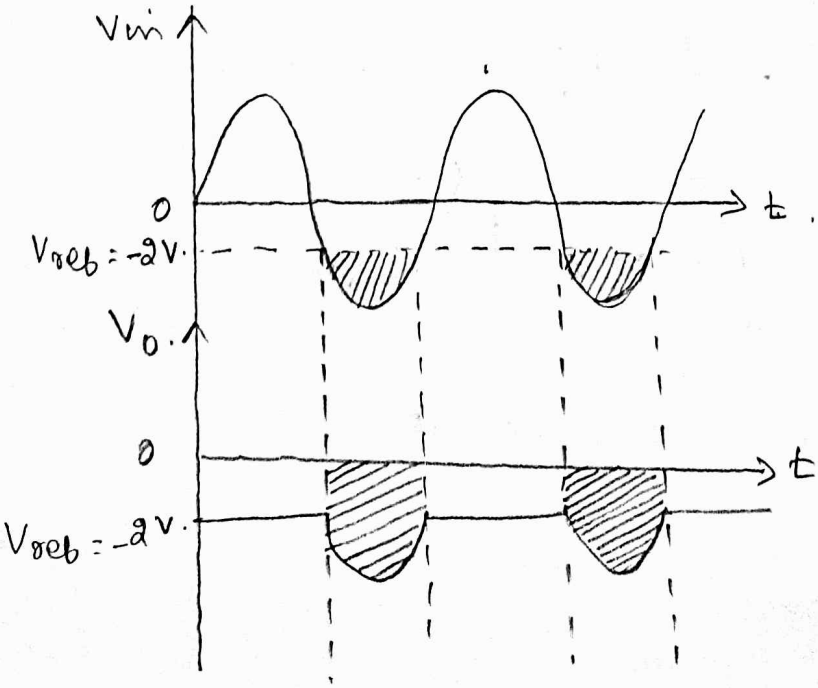
=> In the positive half cycle of the input Vin, the diode D conducts till Vin = Vreb.

=> when Vin < Vreb, Diode D becomes forward biased op-amp acts as a voltage follower. $V_o = V_{in}$.

=> when Vin > Vreb, Diode D becomes reverse biased and open. $V_o = V_{reb}$, the waveform above Vreb gets clipped off.

=> High speed op-amp like HA 2500, LM310, μA 318 used for such applications.

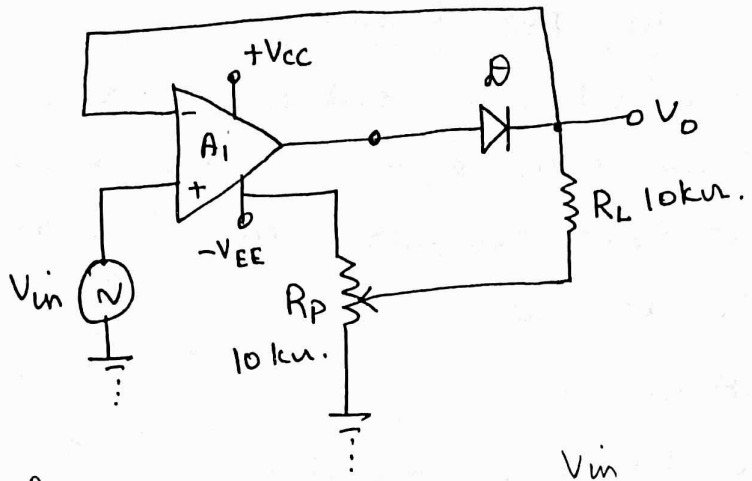
Negative Vreb :-

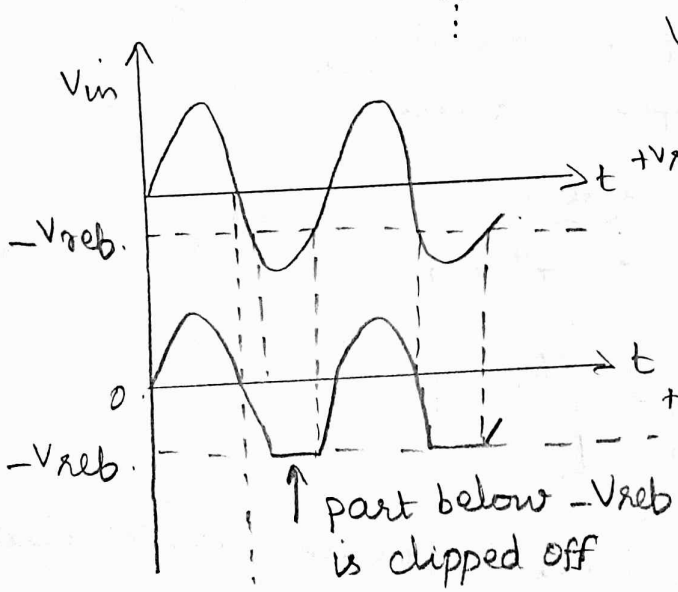


waveforms with negative Vreb.

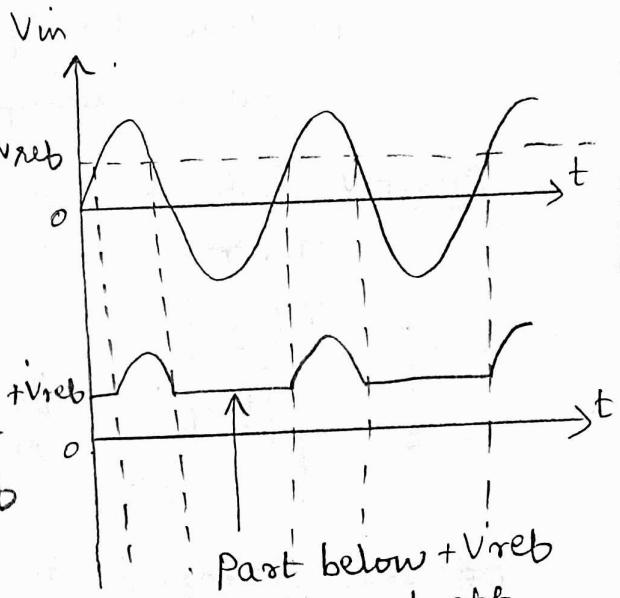
⇒ If the pot R_P is used with $-V_{EE}$ to generate negative V_{reb}. The entire waveforms above $-V_{reb}$ gets clipped off. Let $V_{reb} = -8V$, $V_{in} < -V_{reb}$, i.e $V_{in} < -8V$, the output follows input only.

Negative clipper circuit :-





waveforms with $-V_{reb}$.



waveforms with $+V_{reb}$.

⇒ Negative clipper circuit obtained by reversing the connection of diode D and pot R_P to generate negative reference voltage V_{reb}.

waveforms with $-V_{reb}$:-

When $V_{in} > -V_{reb}$, Diode D conducts, $V_o = V_{in}$.

When $V_{in} < -V_{reb}$, D is off, voltage below $-V_{reb}$ gets clipped off.

waveforms with $+V_{reb}$:-

=) Reference voltage is generated using $+V_{cc}$.
i.e., $+V_{reb}$.

=) $V_{in} > V_{reb}$, D is ON, $V_o = V_{in}$.

=) $V_{in} < V_{reb}$, D is OFF, $V_o = V_{reb}$.

Clamper circuits.

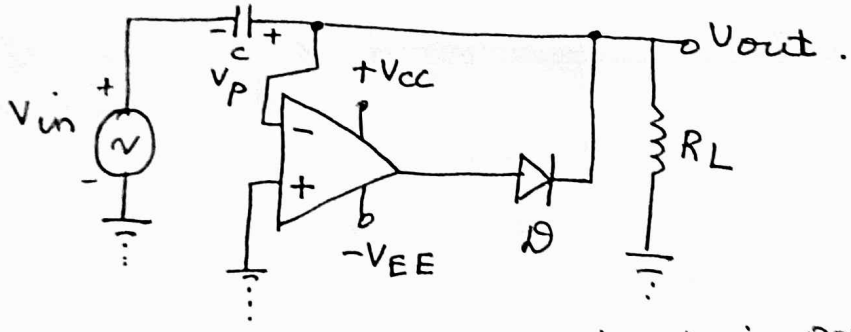
The circuit which are used to add a d.c level as per the requirement, to the a.c output are called as clamper circuits. Also known as d.c restorer circuit.

clarifications :

i) positive clamper circuit.

ii) Negative clamper circuit.

Positive clamper circuit :-

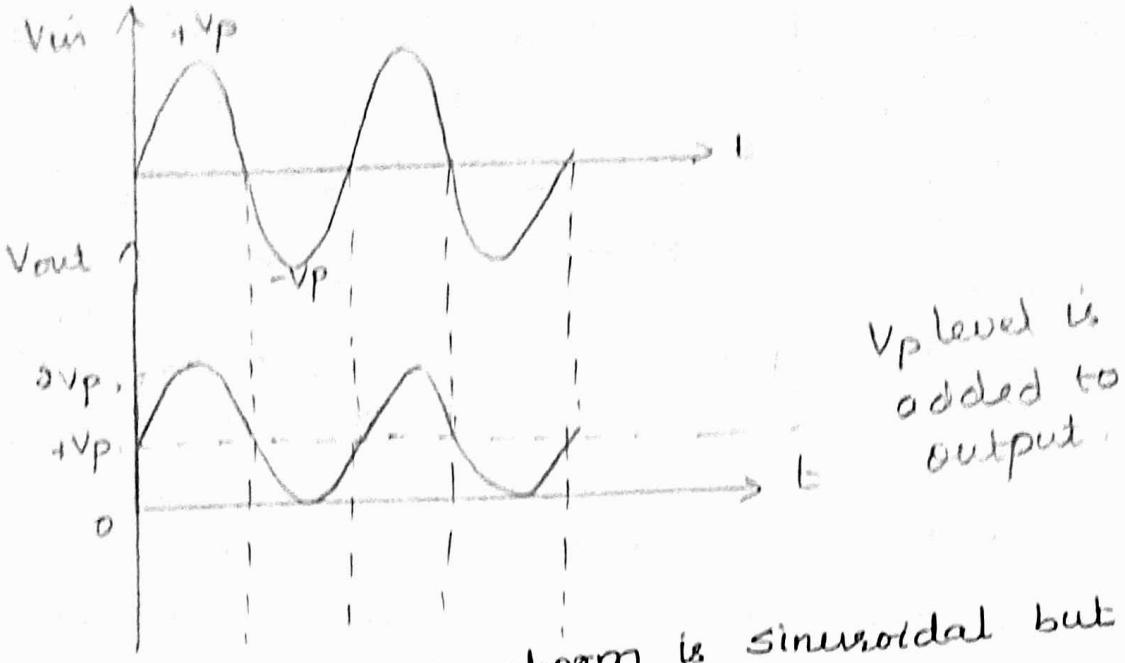


=) If the clamped d.c level is positive, the circuits are called as positive clamper circuits.

=) when the input voltage is first time negative, op-amp output is positive. So, Diode Forward biased. capacitor charges to peak value of the negative cycle of input.

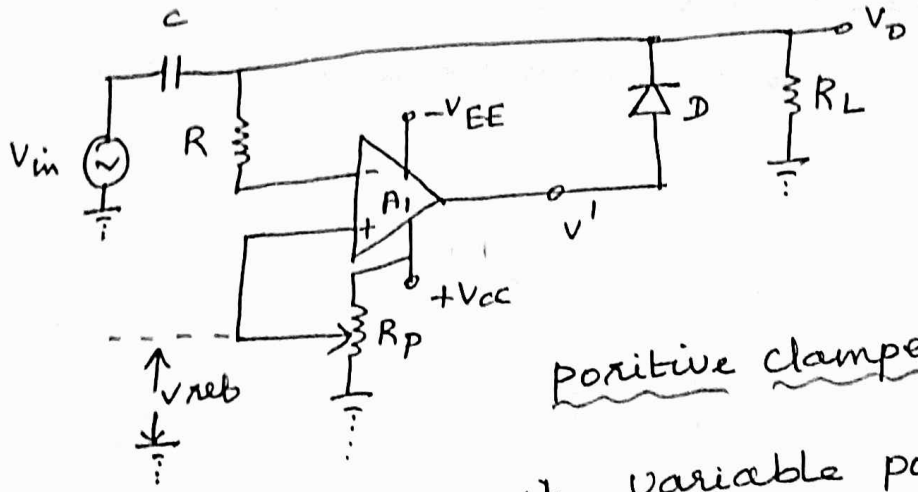
=) Just beyond the negative input peak, diode becomes reverse biased and stops conducting. It becomes open. So, $V_{out} = V_{in} + V_p$.

$V_p \rightarrow$ capacitor voltage.



=> The final output waveform is sinusoidal but shifted positively through Vp.

=> The output waveform swings from 0 to 2Vp (peak to peak voltage of output waveform).



Positive clamper circuit

In the above circuit, variable positive d.c level can be added. The input voltage is applied to the inverting terminal of op-amp A1, variable positive d.c voltage is applied to the non-inverting terminal of the op-amp A1.

=> Apply superposition theorem:

=> Let V_{reb} is acting alone, V_{in} is zero.

=> For positive V_{reb}, output voltage V' is also positive D becomes forward biased. circuit acts as a voltage follower. $V_o = V_{reb}$.

=> Let $V_{in} = V_m \sin \omega t$. (input at inverting terminal purely sinusoidal).

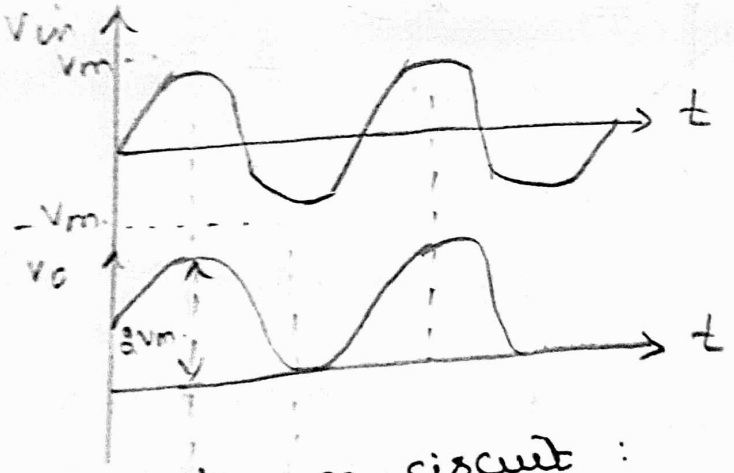
=> For negative half cycle of input, V_o' will rise, D will conduct. capacitor C charges through diode D, to the negative peak voltage V_m.

=> For positive half cycle, diode D does not conduct, C → retains previous voltage V_m.

output voltage $V_o = V_{in} + V_m$.

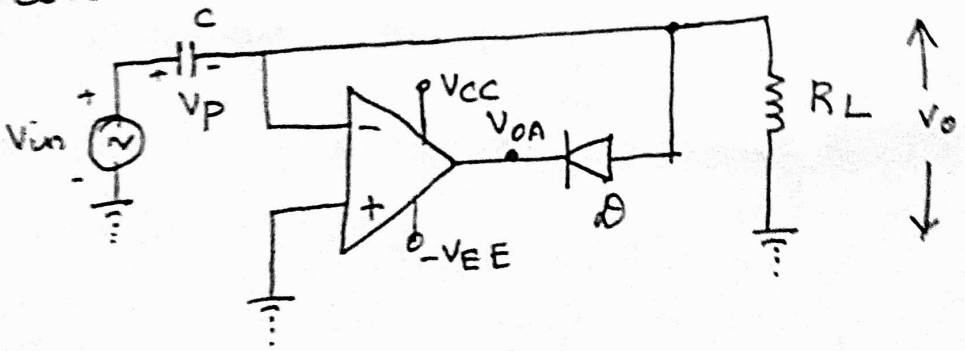
Net output due to both the inputs,

$$V_o = V_{in} + V_m + V_{reb}.$$



Negative clamper circuit:

The clamped d.c level is negative, the circuits are called as negative clamper circuit.



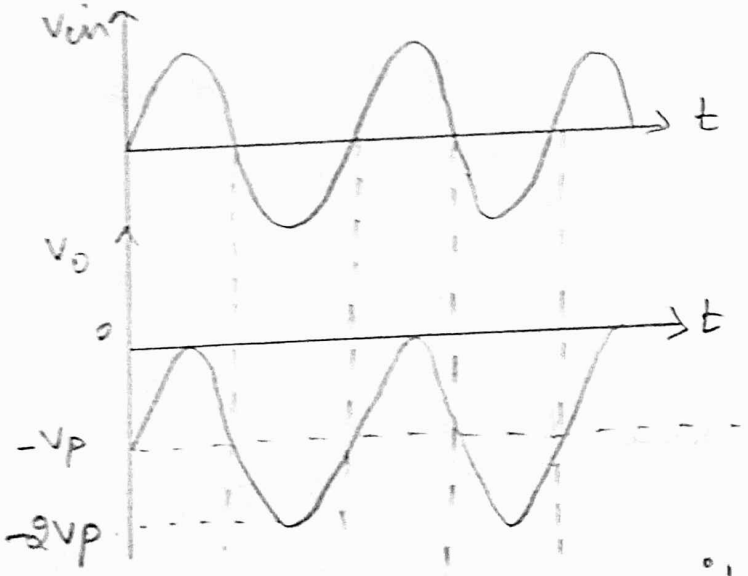
=) Negative clamper circuit obtained by reversing the diode connections in +ve clamper circuit.

=) When V_{in} is first positive going, the voltage V_{OA} goes negative. D becomes Forward biased and capacitor charges to peak value with polarities.

=) Just beyond the positive peak, the diode becomes reverse biased, and becomes open.

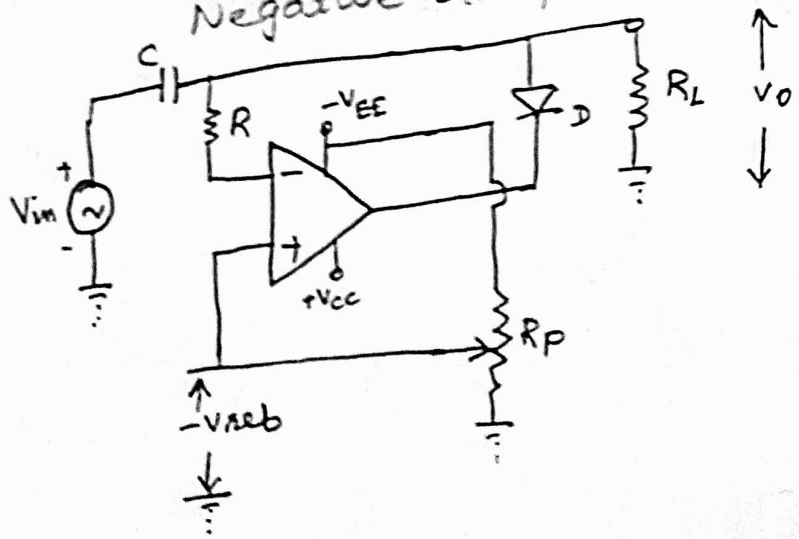
$$V_o = V_{in} - V_p.$$

=) Negative d.c level of $-V_p$ gets added to the output so, the circuit is called negative clamper circuit.



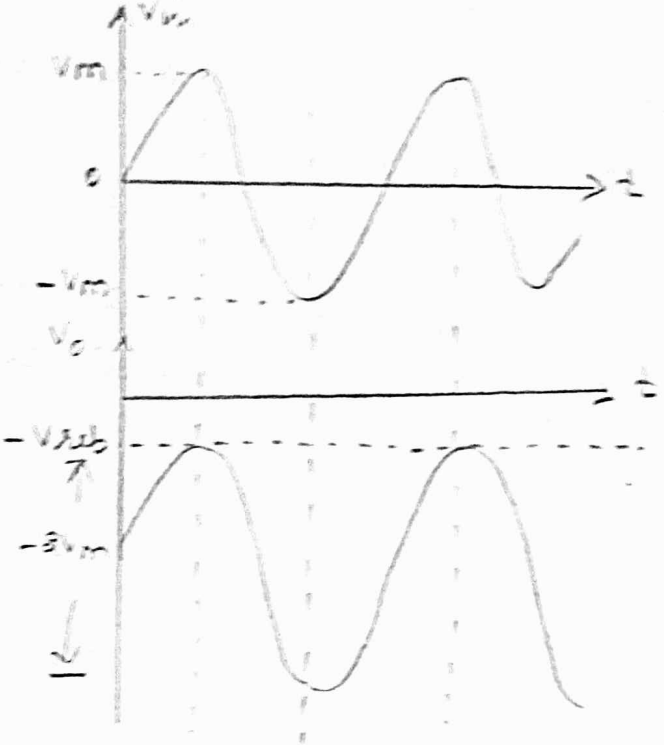
↓ $-V_p$ is added to the output.

Negative clamper circuit.



=) Another circuit in which variable negative d.c level can be added.

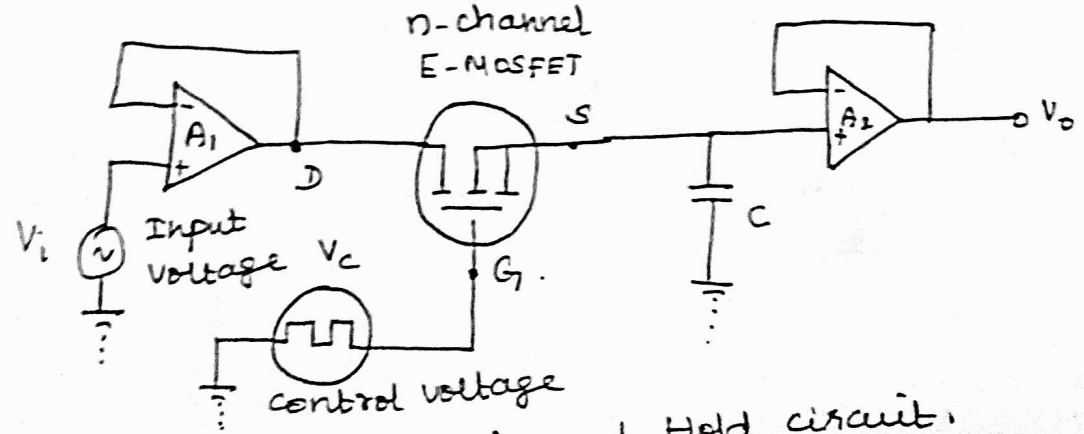
=) $-V_{ref}$ is generated using negative supply $-V_{EE}$.
Diode connections are reversed. So, capacitor charges in reverse direction.



Waveforms for negative clipper.

Sample and Hold circuit :-

=) A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again. This type of circuit is useful in digital interfacing and analog to digital & pulse code modulation systems.



Sample and Hold circuit.

=> The n-channel E-MOSFET works as a switch and is controlled by the control voltage V_C & the capacitor C stores the charge.

=> The analog signal V_i to be sampled is applied to the drain of E-MOSFET and V_C is applid to its gate.

=> when V_C is positive, the E-MOSFET turns on, capacitor C charges to the instantaneous value of input V_i with a time constant $(R_o + r_{DS(ON)})$.

R_o → output resistance of A_1.

$r_{DS(ON)}$ → Resistance of the MOSFET when on.

=> V_i appears across the capacitor C & output through voltage follower A_2.

=> when the V_C is zero, E-MOSFET is off. The capacitor C is now facing the high input impedance of the voltage follower A_2 & cannot discharge. capacitor holds the voltage across it.

Sample period :-

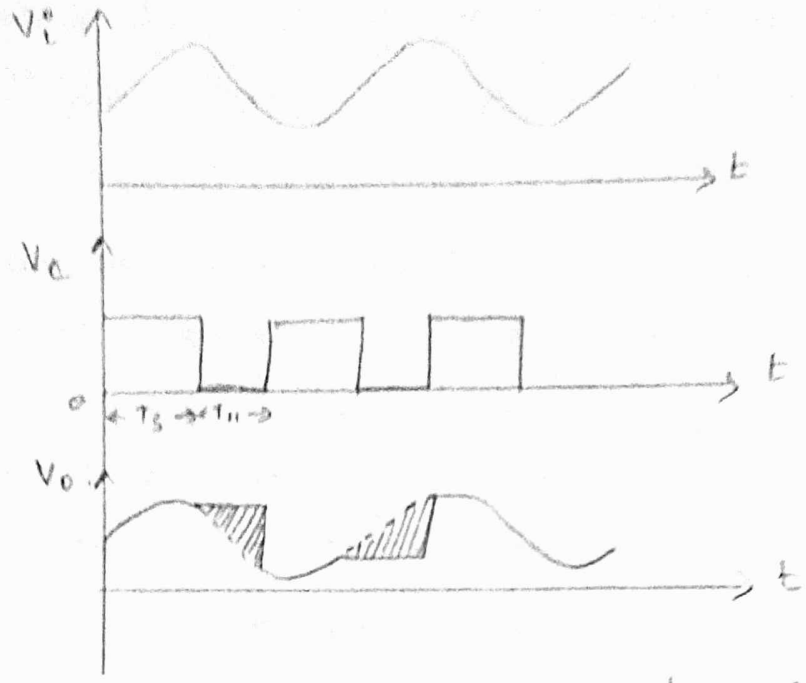
The time period T_s, the time during which voltage across the capacitor is equal to input voltage is called sample period.

Hold period :-

The time period T_H of V_C during which the voltage across the capacitor is held constant is called hold period.

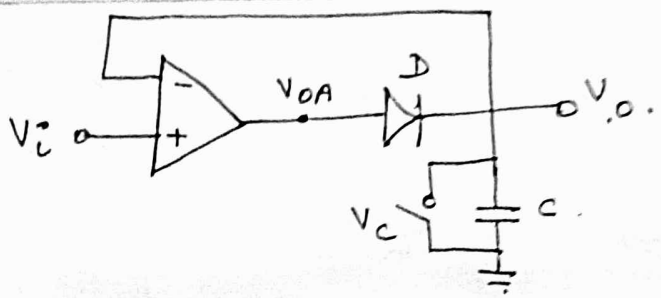
Sample and Hold Ics are,

LF198, LF398.



Input & output waveforms.

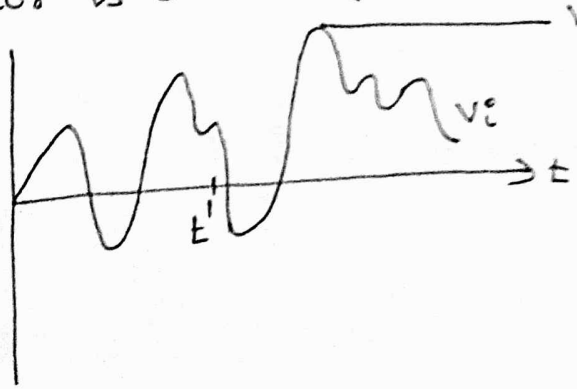
Peak Detector :-



=> The function of peak detector is to compute the Peak value of the input. The circuit follows the voltage peaks of a signal and stores the highest value on a capacitor.

=> If a higher peak signal value comes along, this new value is stored.

=> The highest peak value is stored until the capacitor is discharged.



output V_o corresponding to arbitrary input V_i.

=> When the input V_i exceeds V_c, diode D is forward biased. The circuit becomes voltage follower.

=> The output voltage V_o follows V_i as long as V_i exceeds V_c.

=> When V_i drops below V_c, diode becomes reverse biased, the capacitor holds the charge till input voltage again attains a value greater than V_c.

=> Analysis of waveform :-

① Peak at time t' is missed. The circuit can be reset, V_c can be made zero by connecting a low leakage MOSFET switch across the capacitor.

Applications :-

1) Measurement instrumentation.
2) Amplitude modulation (AM) communication.

D/A converter :-

Weighted Resistor DAC :-

=> Fig shows the summing amplifier with a binary weighted resistor network. It has n electronic switches $d_1, d_2, \ldots, d_n$ controlled by binary input word. There switches are single pole double throw (SPDT) ~~so~~ type.

=> If the input bit is 0, switch connects the resistor to the ground.

output current $I_O = I_1 + I_2 + \ldots + I_n$.

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots + \frac{V_R}{2^n R} d_n.$$

$$= \frac{V_R}{R} \left[d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n} \right).$$

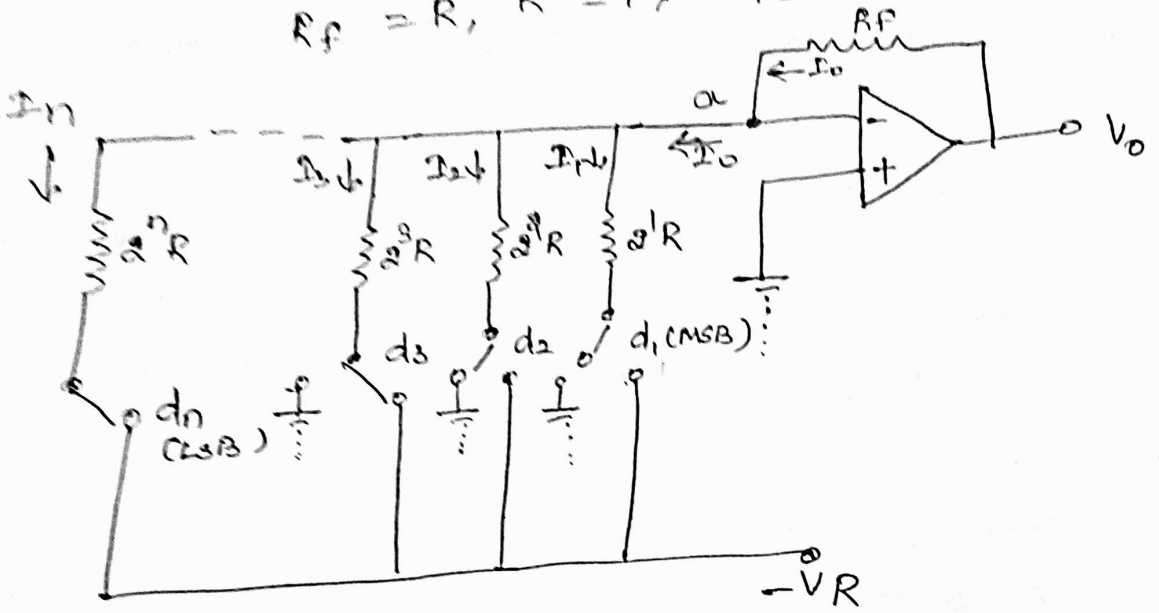
Output voltage $V_0 = I_0 R_f$

$= V_R \frac{R_f}{R} (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n})$ —(1)

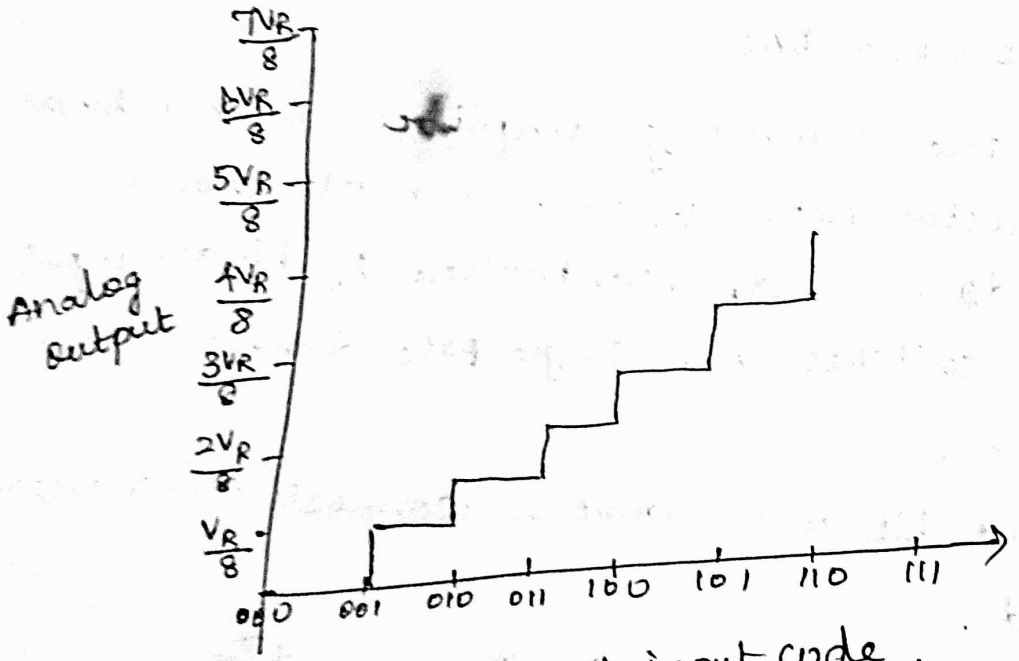
$V_0 = K V_{FS} (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n})$ —(2)

Compare (1) & (2),

$R_f = R$, $K = 1$, $V_{FS} = V_R$.

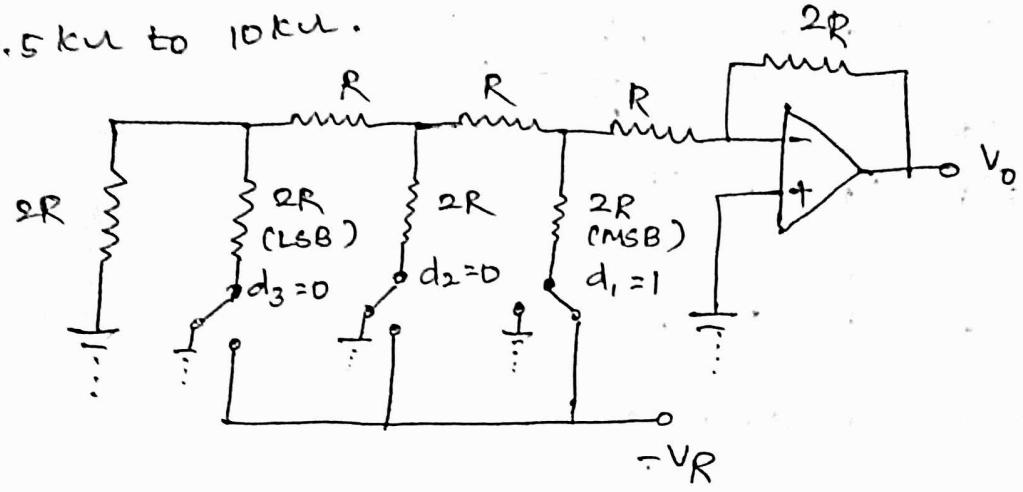


Simple weighted resistor DAC.

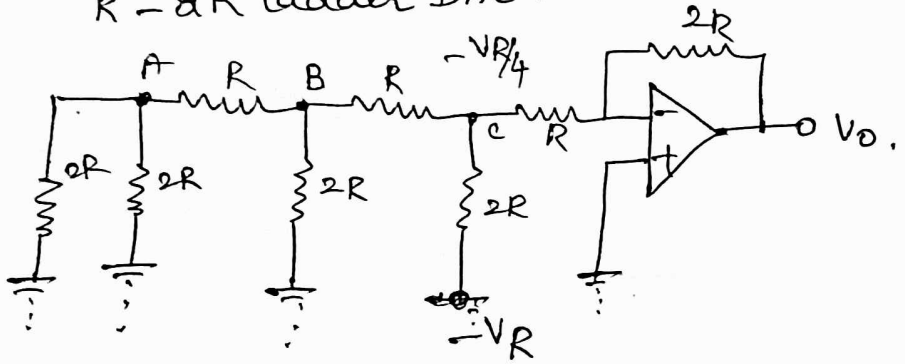


R-2R ladder DAC :-

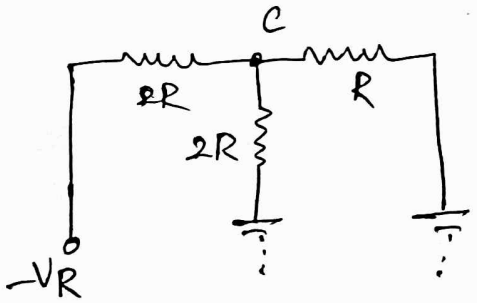
⇒ Wide range of resistors are required in binary weighted resistor type DAC. Only two values of resistors are required. Typical value of R ranges from 2.5 kΩ to 10 kΩ.



R-2R ladder DAC.



Equivalent circuit (b)



equivalent circuit of (b).

3 bit DAC shown in fig. switch position d_1, d_2, d_3 corresponds to the binary word 100.

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R + 2/3\,R} = -V_R/4 .$$

$$V_o = \frac{-2R}{R}\left(\frac{-V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2} .$$

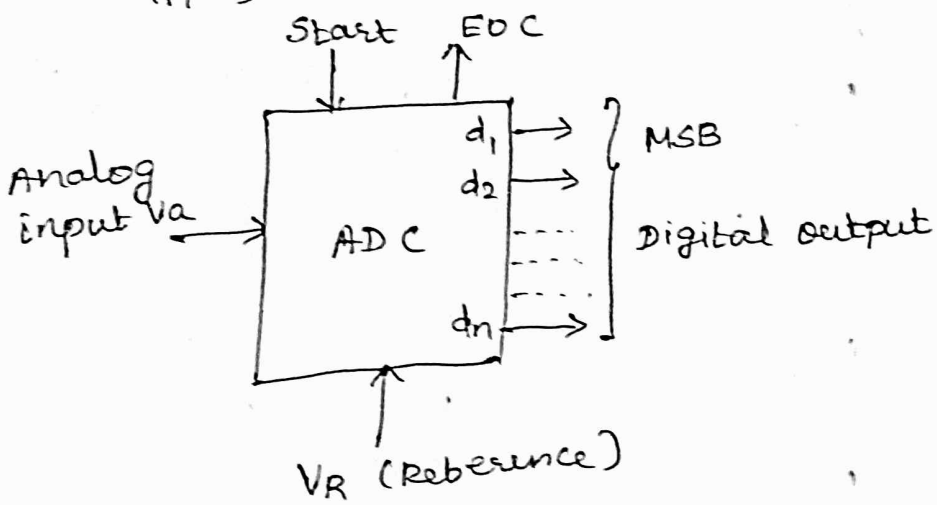
A-D Converters :-

It accepts an analog input voltage V_a and produces an output binary word $d_1, d_2, \ldots d_n$ of functional value D,

$$D = d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}$$

$d_1 \rightarrow$ Most significant Bit

$d_n \rightarrow$ Least significant Bit.



Functional Diagram of ADC.

START → Tell the ADC when to start the conversion.

EOC → End of conversion.

i) Direct type ADCs.

ii) Integrating type ADCs.

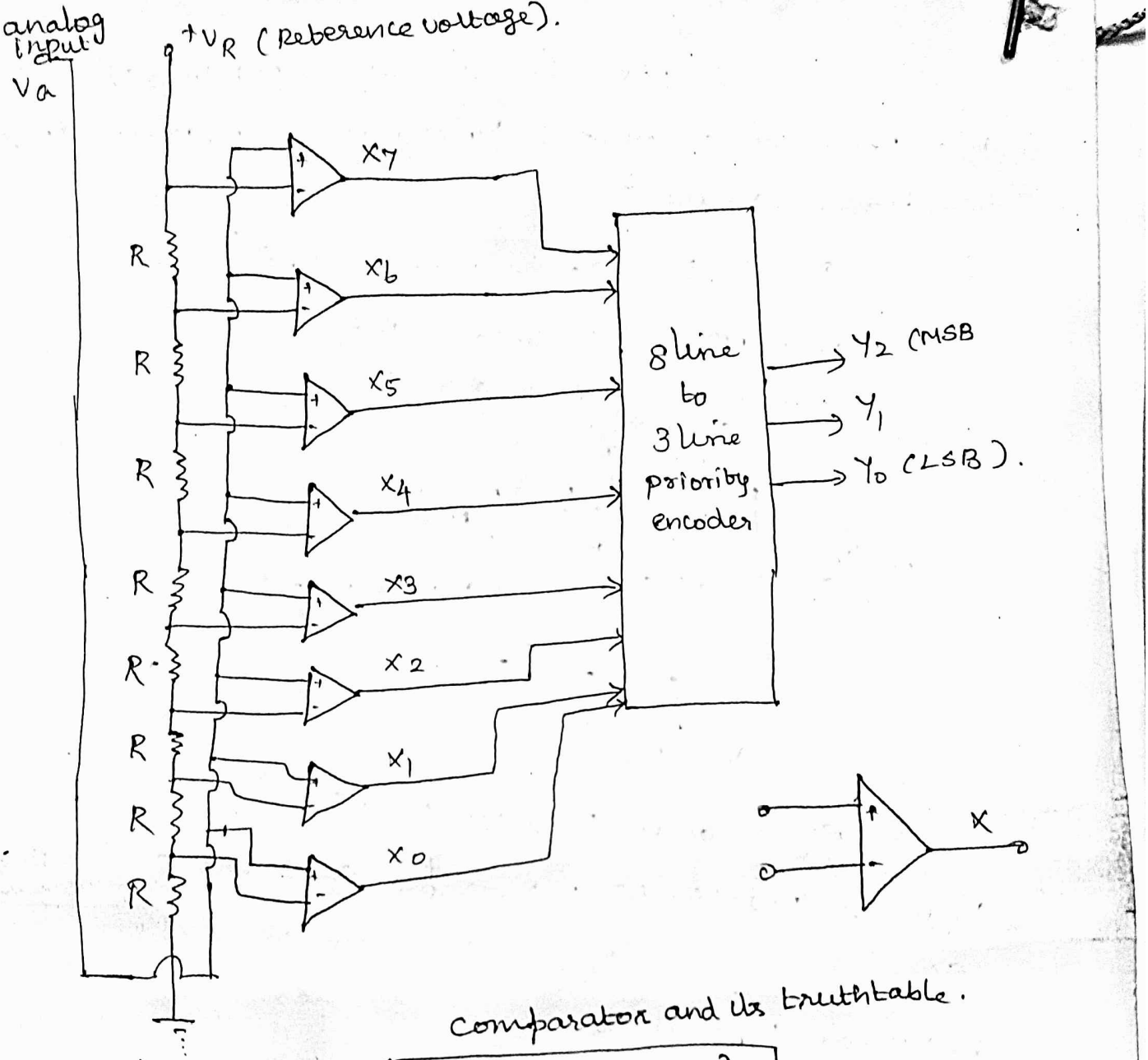
Direct type ADCs :-

=> Simplest possible A/D converter.

=> The circuit consists of resistive divider network, 8 op-amp comparators, 8 line to 3 line encoder.

=> All the resistors are of equal value, the voltage levels available at the nodes are equally divided between the V_R and ground.

The switch position in Analog line



Comparator and its truth table.

Voltage input	Logic output (x)
Va > Vd	x = 1
Va < Vd	x = 0
Va = Vd	previous value

Truth table for flash type A/D. Converter

Input voltage Va	X7	X6	X5	X4	X3	X2	X1	X0	Y2	Y1	Y0
0 to VR/8	0	0	0	0	0	0	0	1	0	0	0
VR/8 to VR/4	0	0	0	0	0	0	1	1	0	0	1
VR/4 to VR/8	0	0	0	0	0	1	1	1	0	1	0
3VR/8 to VR/2	0	0	0	0	1	1	1	1	0	1	1
VR/2 to 5VR/8	0	0	0	1	1	1	1	1	1	0	0
5VR/8 to 3VR/4	0	0	1	1	1	1	1	1	1	0	1
3VR/4 to 7VR/8	0	1	1	1	1	1	1	1	1	1	0
7VR/8 to VR	1	1	1	1	1	1	1	1	1	1	1

UNIT - IV

SPECIAL ICs

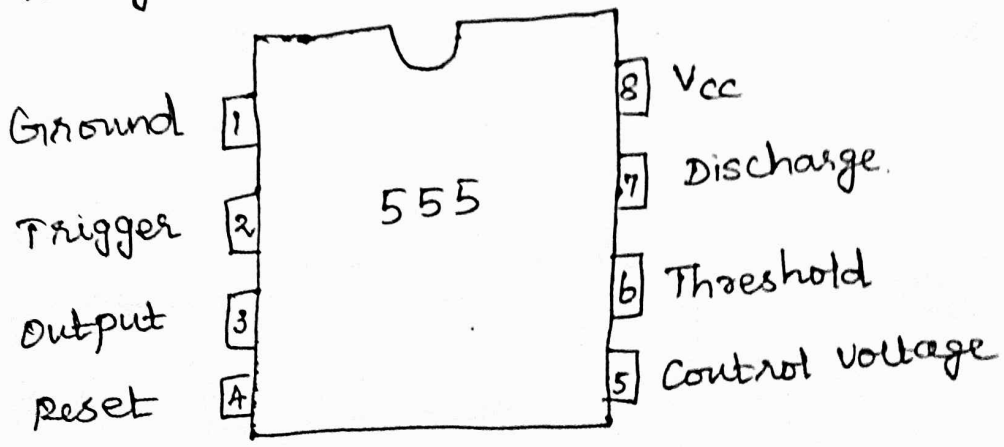
Functional Block, characteristics of 555 Timer and its PWM application. IC 566 voltage controlled oscillator IC : 565 - Phase locked loop IC, AD 633 Analog multiplier ICs.

555 Timer :-

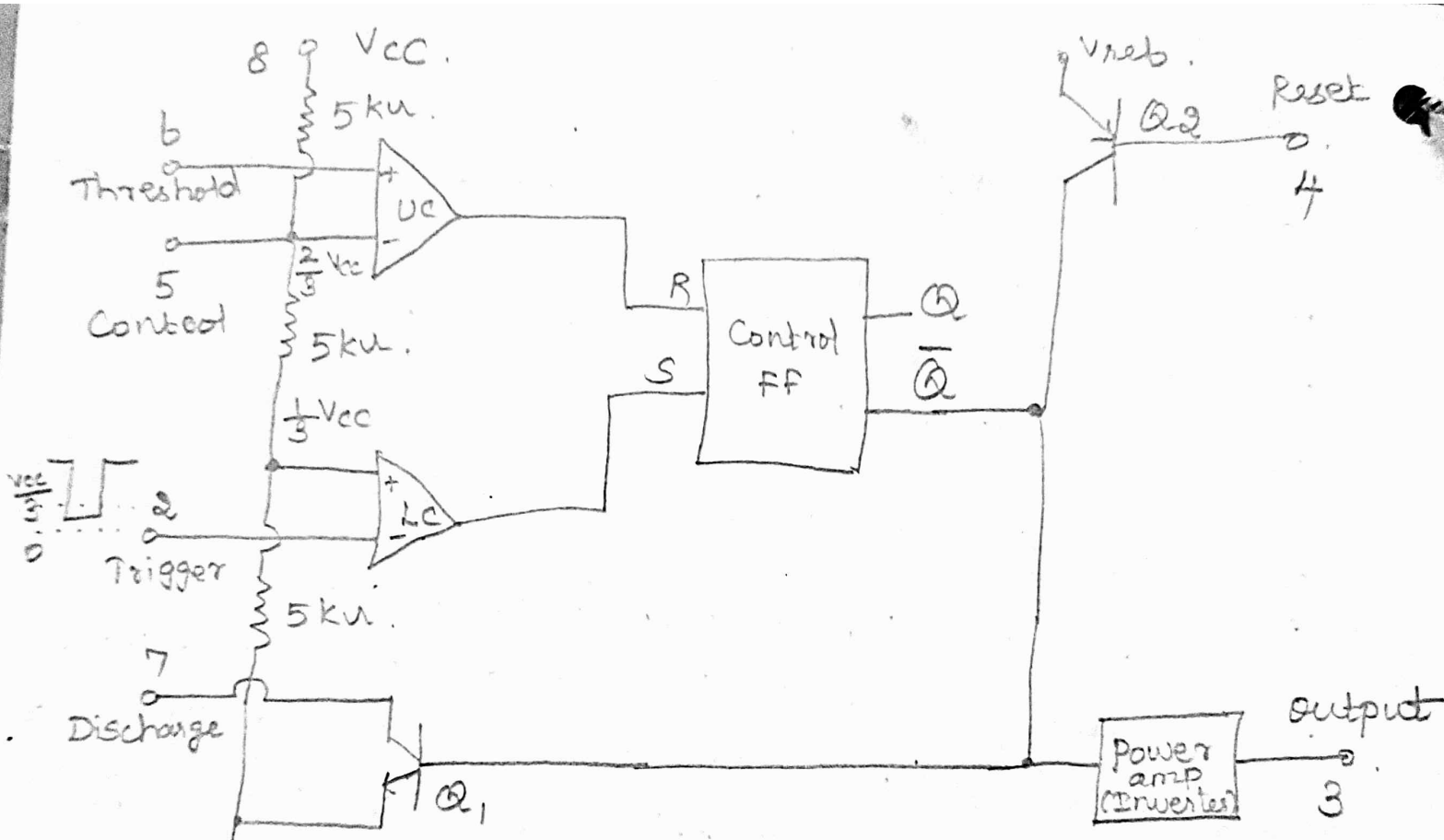
The 555 timer is a highly stable device for generating accurate time delay or oscillation. It can provide time delay ranging from microseconds to hours. used with supply voltage in the range of +5V to +18V, and drive load upto 200mA.

Applications :-

1) oscillator
2) Pulse Generator
3) Ramp and square wave generator.
4) Mono-shot multivibrator
5) Burglar Alarm
6) Traffic light control
7) Voltage Monitor.



8 Pin Package - Pin Diagram.



Functional Diagram of 555 Timer.

The functions of 555 Timer IC :

Pin 1 : Ground

All the voltages are measured with respect to this terminal.

Pin 2 : Trigger

The 555 timer IC uses two comparators. The voltage divider consists of 3 equal resistances. Due to voltage divider, the voltage at inverting terminal of comparator is biased at $\frac{V_{cc}}{3}$, when the trigger input is slightly less than $\frac{V_{cc}}{3}$, the comparator output goes high. This output is given to reset input of flip flop. So high output of comparator resets the flip-flop.

Pin 3 : output :-

The complementary signal output is given to pin 3 which is the output. The load can be connected in two ways. i) Between pin 3 & ground
ii) Between pin 3 & V_{cc}.

Pin 4 : Reset :-

When pin 4 is grounded, it stops the working of device and makes it OFF. Pin 4 provides on/off feature to 555 Timer IC.

Pin 5 : Control voltage Input :-

⇒ Inverting input terminal of comparator 1. The voltage divider holds the voltage of this input at 2/3 V_{cc}.

Pin 6 : Threshold

⇒ Noninverting input terminal of comparator 1. External voltage is applied to this pin 6. When this voltage is more than 2/3 V_{cc}, comparator 1 output goes high. This is given to the set input of R-S flip-flop. The high output of comparator 1 sets the flip-flop. This makes Q of flip-flop high & $\bar{Q}$ low. Output at pin 3 goes low.

Threshold > $\frac{2}{3}$ V_{cc}, flip-flop → set, Q → high
output → low.

Trigger < 1/3 V_{cc}, flip flop → reset, Q → low,
output - high.

Pin 7 : Discharge :

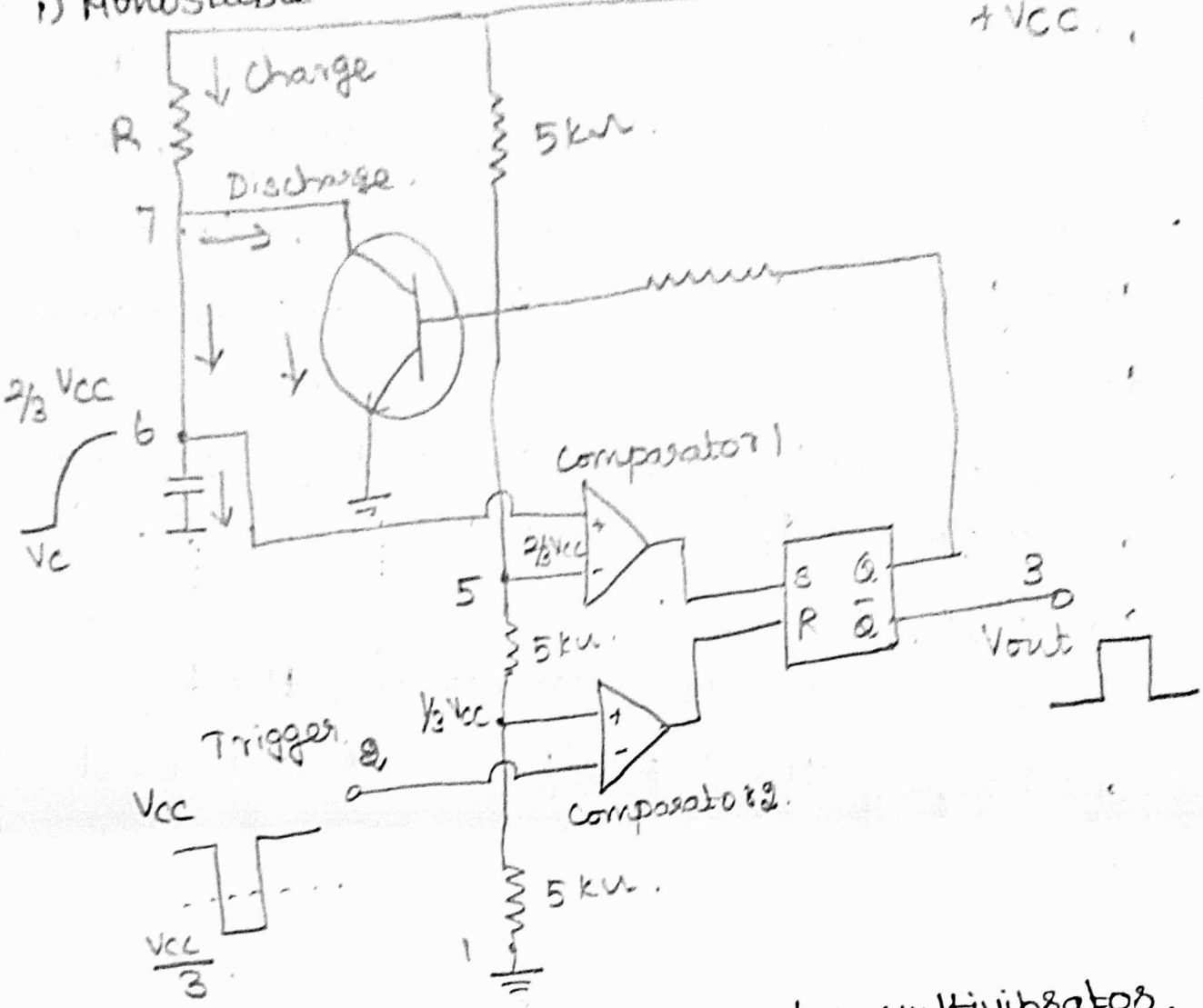
This pin is connected to collector of the discharge transistor Qd. When output is high, Q is low, Qd - off. It acts as an open circuit. When output low, Q is high, drives the base of Qd high. Transistor acts as an short circuit.

Pin 8 : Power supply.

IC 555 work with supply voltage b/w 4.5 V & 16V.

PWM Applications :-

1) Monostable Multivibrator using IC 555 :-



=) It is often called a one-shot multivibrator.

=) It is a pulse generator circuit in which the duration of the pulse is determined by the R-C network connected externally to 555 timer.

=) It has only one stable state.

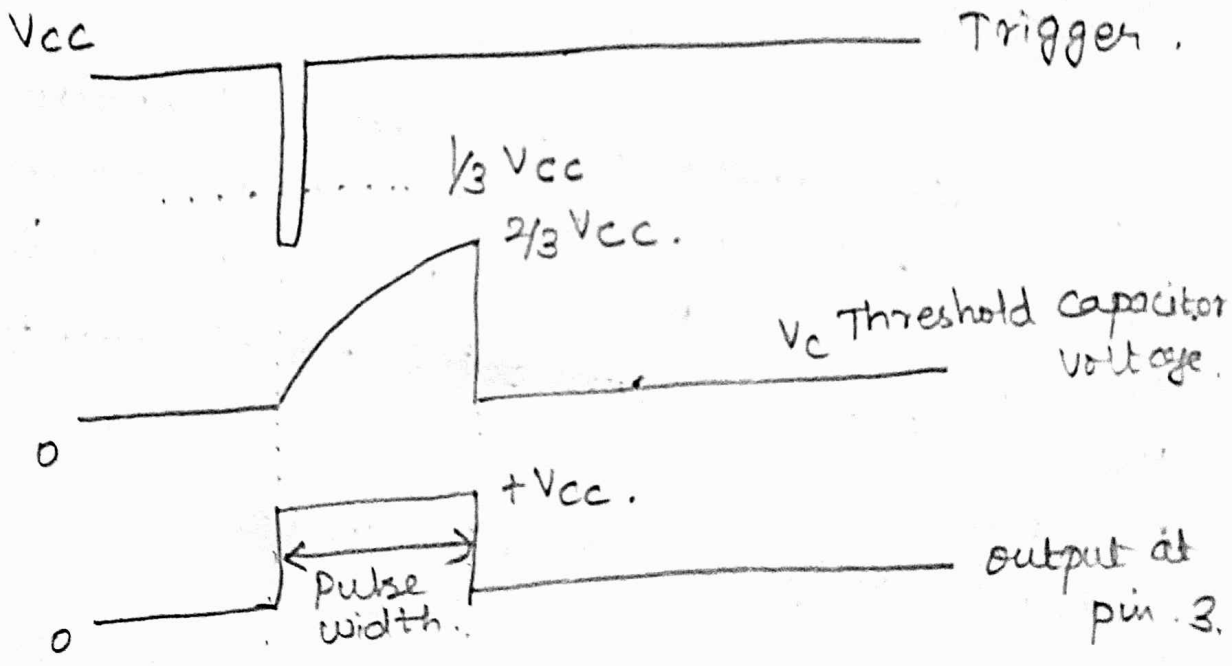
Operation :-

1) Initially when the output at pin 3 is low, the transistor is ON, capacitor C is shorted to ground.

=) when a negative pulse is applied to pin 2, trigger input falls below $\frac{Vcc}{3}$, comparator 2 goes high, which resets the flip-flop. The transistor turns off, output at pin 3 goes high.

=) The capacitor C begins charging toward +Vcc through R with a time constant equal to RC.

=) when increasing capacitor voltage slightly greater than $\frac{2}{3}$ Vcc, output of comparator 1 goes high, which sets the flip-flop. The transistor goes to saturation, thereby discharging the capacitor C and output goes low.



Trigger input, Output voltage, capacitor voltage waveforms.

Derivation of pulsewidth :-

The voltage across the capacitor increases exponentially and is given by,

$$V_c = V\left(1 - e^{-t/RC}\right).$$

$$V_c = 2/3\, V_{cc}.$$

$$2/3\, V_{cc} = V_{cc}\left(1 - e^{-t/RC}\right).$$

$$2/3 - 1 = -e^{-t/RC},$$

$$1/3 = e^{-t/RC},$$

$$-\frac{t}{CR} = -1.0986.$$

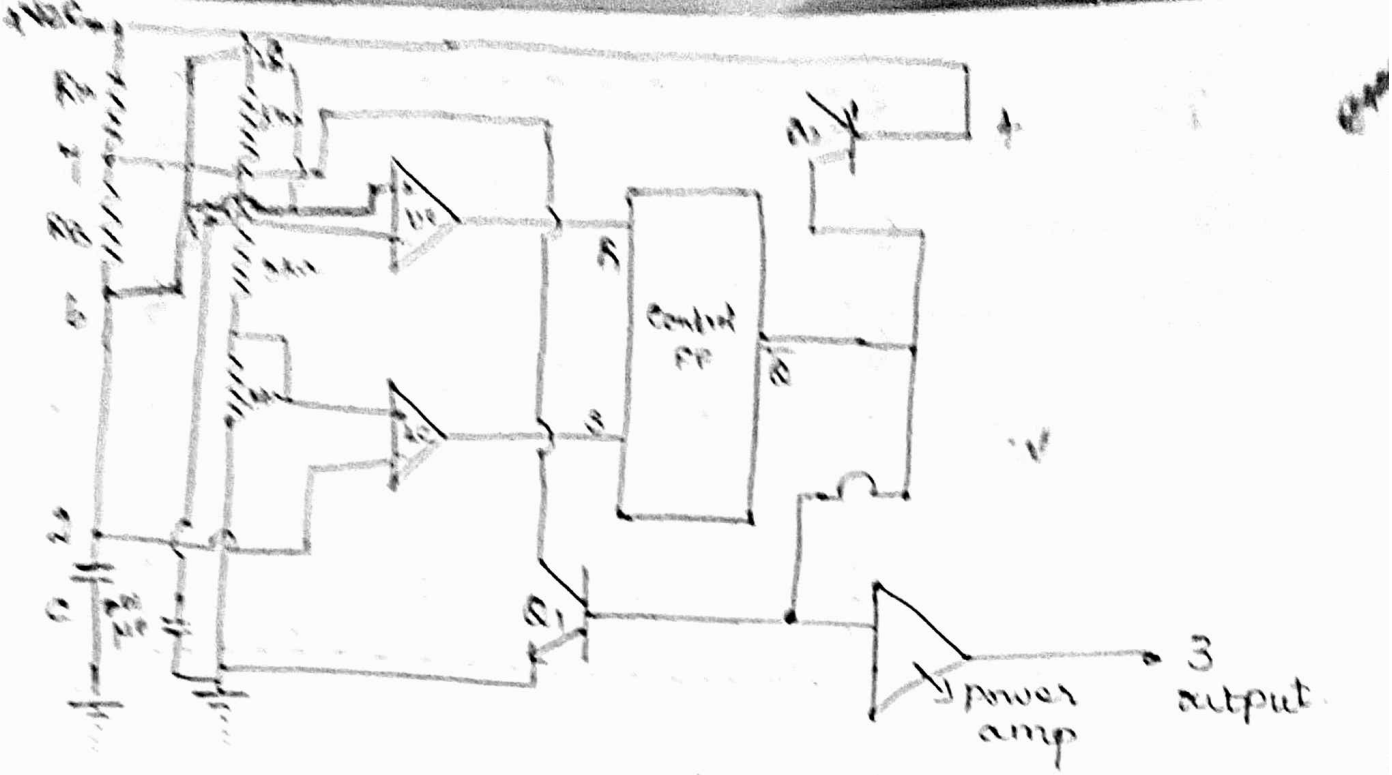
$$t = +1.0986\, RC.$$

$$\boxed{t = 1.1\, CR}$$

Astable Multivibrator using IC 555 :-

An astable multivibrator often called a free-running multivibrator, is a rectangular wave generating circuit.

It does not require any external trigger to change the state of the output, hence the name free-running.



Astable Multivibrator using 555 timer.

Operation :-

When the flip-flop is set, Q is high which drives the transistor Q1 in saturation and the capacitor gets discharged.

⇒ Now the capacitor voltage is nothing but the trigger voltage. While discharging, when it becomes less than $\frac{V_{cc}}{3}$, comparator 2 output goes high.

⇒ This resets the flip-flop hence Q goes low, and $\bar{Q}$ goes high. This low Q makes the transistor Q1 off. The capacitor starts charging through the resistances R_A, R_B & V_{cc}.

charging time constant $(R_A + R_B)C$.

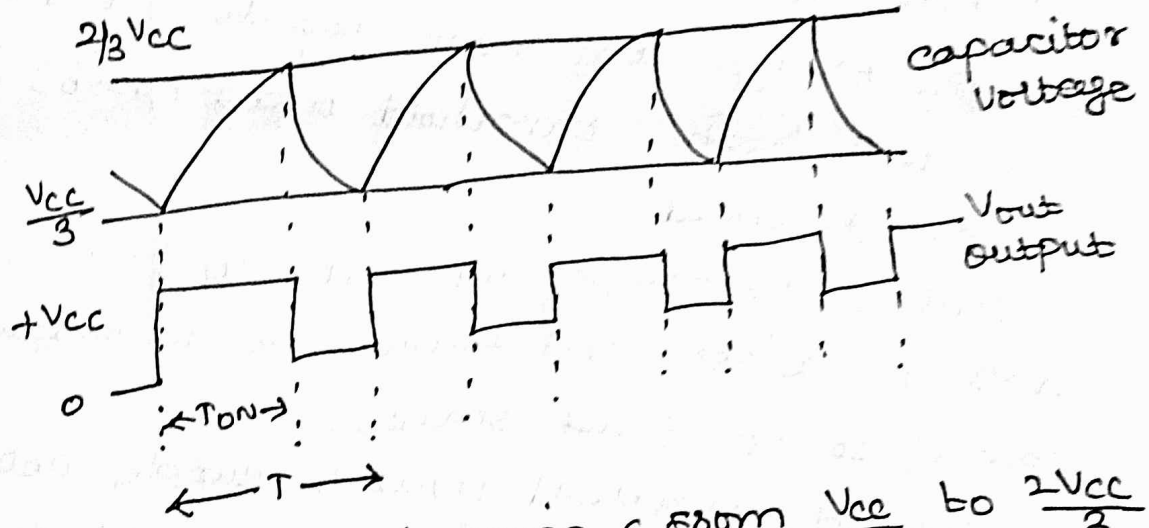
⇒ Now capacitor voltage is also a threshold voltage. while charging, capacitor voltage

increases, the threshold voltage increases.

⇒ when it exceeds $\frac{2}{3}V_{CC}$, comparator 1 output goes high which sets the flip-flop. The flipflop output Q becomes high and output at pin 3 $\bar{Q}$ becomes low.

⇒ High Q drives transistor Qd in saturation and capacitor starts discharging through resistance RB and transistor Q.d.

⇒ when capacitor voltage less than $\frac{V_{CC}}{3}$ comparator 2 output goes high, Resets the flip-flop. This cycle repeats.



The time for charging C from $\frac{V_{CC}}{3}$ to $\frac{2V_{CC}}{3}$

T_C = ON time = 0.693 $(R_A + R_B)$ C.

The time for discharging C from $\frac{2V_{CC}}{3}$ to $\frac{V_{CC}}{3}$,

T_d = Off time = 0.693 RB. C.

Total oscillation period,

$T = T_C + T_d = 0.693 (R_A + R_B).C + 0.693 R_B C.$

$T = 0.693 (R_A + 2R_B) \times C.$

$f = \frac{1}{T_{OSC}} = \frac{1.44}{(R_A + 2R_B)C}$.

+Vcc

RB

Duty cycle = $R_A + R_B / R_A + 2 \cdot R_B$.

$$f_{osc} = \frac{1}{T_{osc}} = \frac{1.44}{(R_A + R_B) \cdot C}$$

Applications of 555 timer in astable mode:

1) Schmitt Triggers.
2) Voltage controlled oscillator.
3) FSK Generator.

Bistable Multivibrator :-

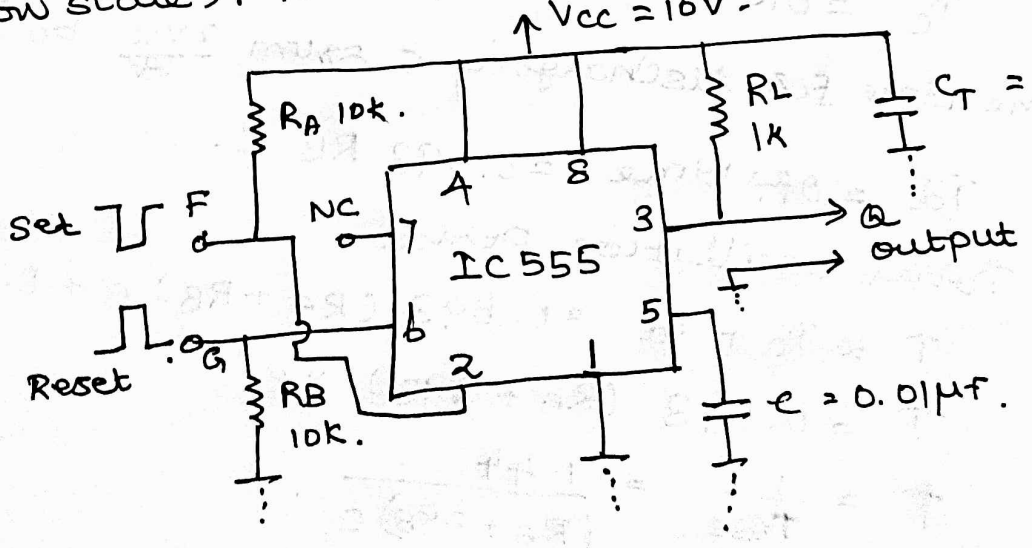
=> In these circuits the output is stable in both the states. The states are switched using an external trigger.

=> There are no RC timing network.

=> The trigger and resets inputs (pin 8 & 4) are held high, threshold input (pin 6) is simply grounded.

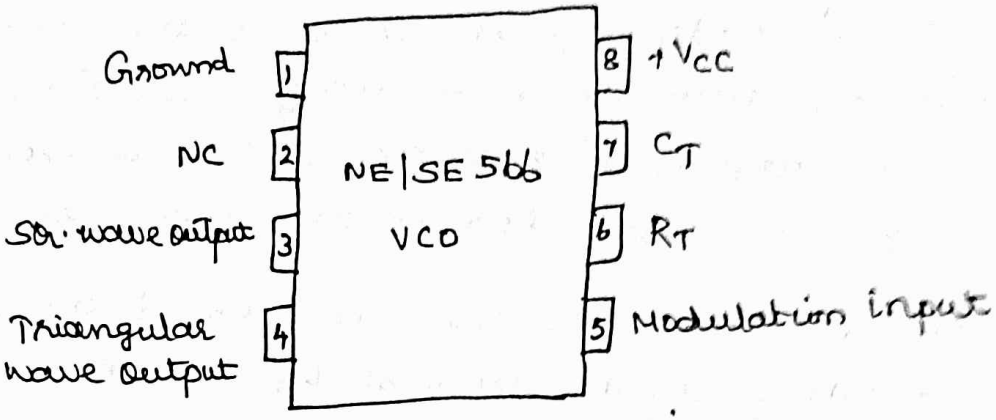
=> Pulling the trigger momentarily to ground acts as a "set" and transitions the output pin (pin 3) to Vcc (high state).

=> Pulling the threshold input to supply acts as a reset and transitions the output pin to ground (low state). No capacitors are required.

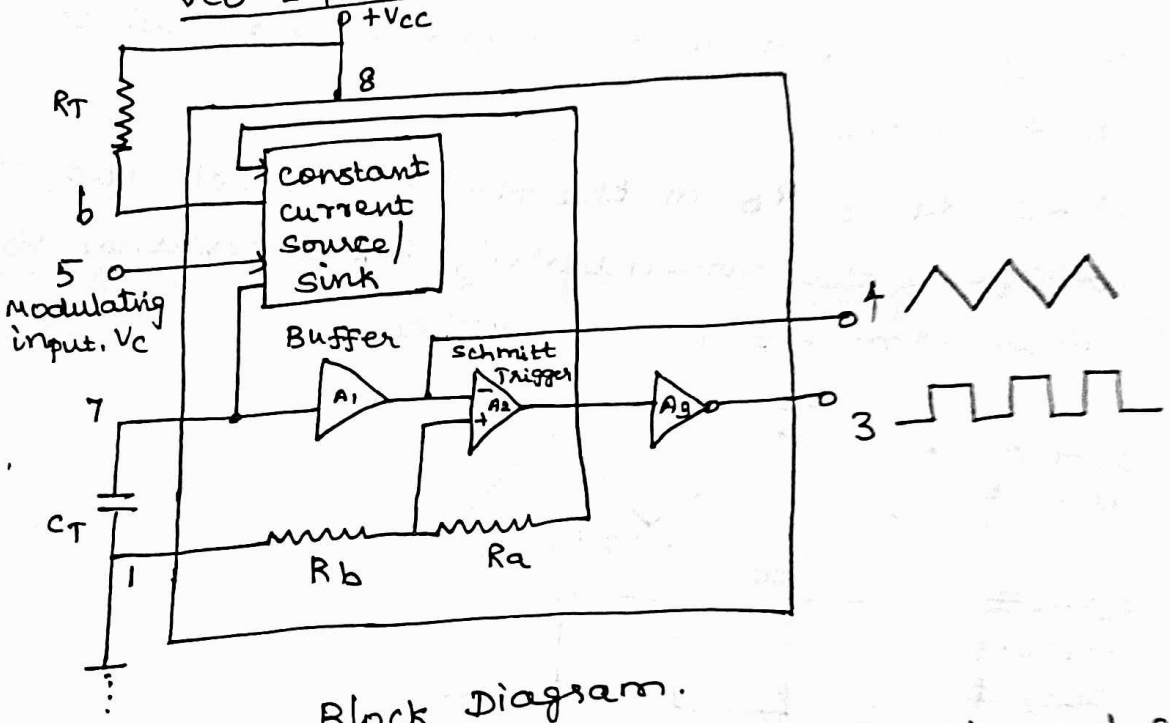


Voltage Controlled oscillator (VCO)

⇒ A common type of VCO available in IC form is Signetics NE/SE 566.



VCO - Pin Configuration



Block Diagram.

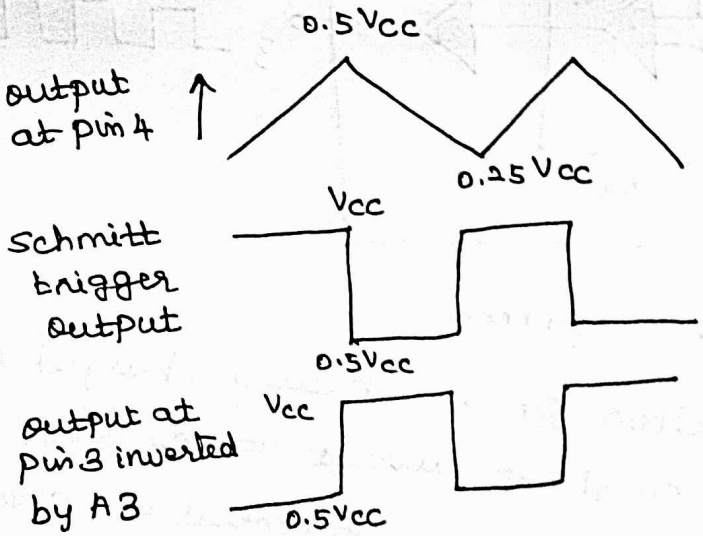
The timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage Vc applied at the modulation input (pin 5).

⇒ The voltage at pin 6 is held at the same voltage as pin 5, or by changing the timing resistor R_T external to IC chip.

* A small capacitor of 0.001 μF should be connected between pin 5 & 6 to eliminate possible oscillations.
* A VCO is used in converting low frequency signals such as EEGs, EKG into an audio frequency range. These audio signals can be transmitted over telephone lines or a two way radio communication system for diagnostic purposes or can be recorded on a magnetic tape for further reference.

⇒ The voltage across the capacitor C_T is applied to the inverting input terminal of schmitt trigger A_2 via buffer amplifier A_1. The output voltage swing of the schmitt trigger is designed to V_{cc} & $0.5V_{cc}$.

⇒ If $R_a = R_b$ in the +ve feedback loop, the voltage at the non-inverting input terminal of A_2 swings from $0.5V_{cc}$ to $0.25V_{cc}$.



output waveform.

⇒ When the voltage on the capacitor C_T exceeds $0.5V_{cc}$ during charging, the output of the schmitt trigger goes low ($0.5V_{cc}$).
⇒ The capacitor now discharges and when it is at $0.25V_{cc}$, the output of schmitt trigger goes high (V_{cc}).

source current & sink current are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across pin 4.

⇒ The square wave output of the schmitt trigger is inverted (inverter is a current amplifier to drive the load), by inverter A3 and available at pin 3.

Output frequency of VCO :-

The total voltage on the capacitor changes from $0.25V_{cc}$ to $0.5V_{cc}$.

$$\Delta V = 0.25 V_{cc}.$$

The capacitor charges with a constant current source

$$\frac{\Delta V}{\Delta t} = \frac{i}{C_T}.$$

$$\frac{0.25V_{cc}}{\Delta t} = \frac{i}{C_T}.$$

$$\Delta t = \frac{0.25 V_{cc} C_T}{i}$$

The time period T of the triangular waveform $= 2\Delta t$.

The frequency of oscillator f_o is,

$$f_o = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{i}{0.5 V_{cc} C_T}.$$

$$i = \frac{V_{cc} - V_c}{R_T}$$

$V_c \rightarrow$ voltage at pin 5,

$$f_o = \frac{V_{cc} - V_c}{0.5 V_{cc} C_T R_T}$$

$$f_o = \frac{2(V_{cc} - V_c)}{C_T R_T V_{cc}} \quad \text{— (I)}.$$

with no modulating input signal, if the voltage at pin 5 is biased at 7/8 V_{cc}, then

Then equation (I) becomes,

$$f_o = \frac{2(V_{cc} - (1/2)V_{cc})}{C_T R_T V_{cc}} = \frac{1}{1.4 R_T C_T} = \frac{0.85}{R_T C_T} \Rightarrow (II)$$

Voltage to frequency conversion factor :-

Voltage to frequency conversion factor K_V is,

$$K_V = \frac{\Delta f_o}{\Delta V_c}$$

Assume original frequency f_o, new frequency f_1.

$$\Delta f_o = f_1 - f_o = \frac{2(V_{cc} - V_c + \Delta V_c)}{C_T R_T V_{cc}} - \frac{2(V_{cc} - V_c)}{C_T R_T V_{cc}}$$

$$= \frac{2\Delta V_c}{C_T R_T V_{cc}}$$

$$\Delta V_c = \frac{\Delta f_o C_T R_T V_{cc}}{2}$$

putting the value of $C_T R_T$ from eqn (II),

$$\Delta V_c = \frac{\Delta f_o}{K_V} = \frac{\Delta f_o \, 0.85 \, V_{cc}}{2 f_o} \qquad \left[\because R_T C_T = \frac{0.25}{f_o}\right]$$

$$= \frac{\Delta f_o V_{cc}}{2.5 f_o}$$

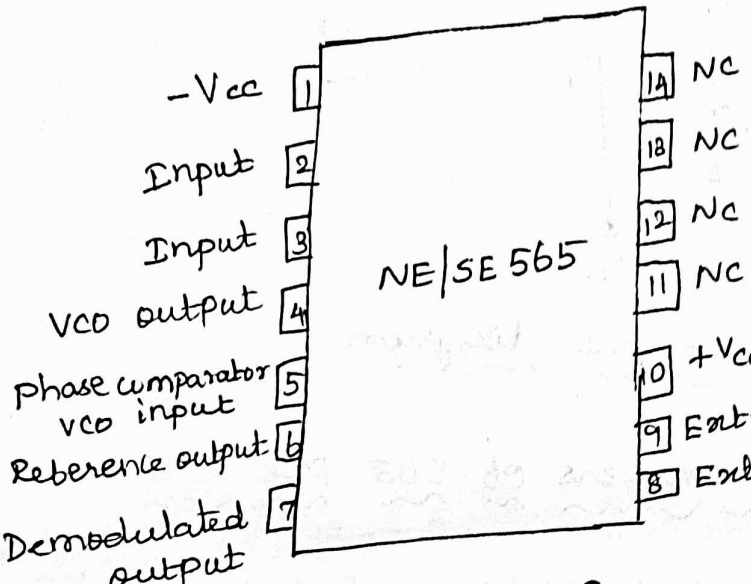
$$\boxed{K_V = \frac{\Delta f_o}{\Delta V_c} = \frac{2.5 f_o}{V_{cc}}} \quad \text{---(III)}$$

Phase Locked Loop (PLL)

⇒ Some important monolithic PLLs are SE/NE 560 series introduced monolithic PLLs. (Signetics)

⇒ The SE/NE 560, 561, 562, 564, 565 & 567 mainly differ in operating frequency range.

⇒ SE/NE 565 is the most commonly used PLL.



Pin Diagram

⇒ 565 is available as a 14 pin DIP package.

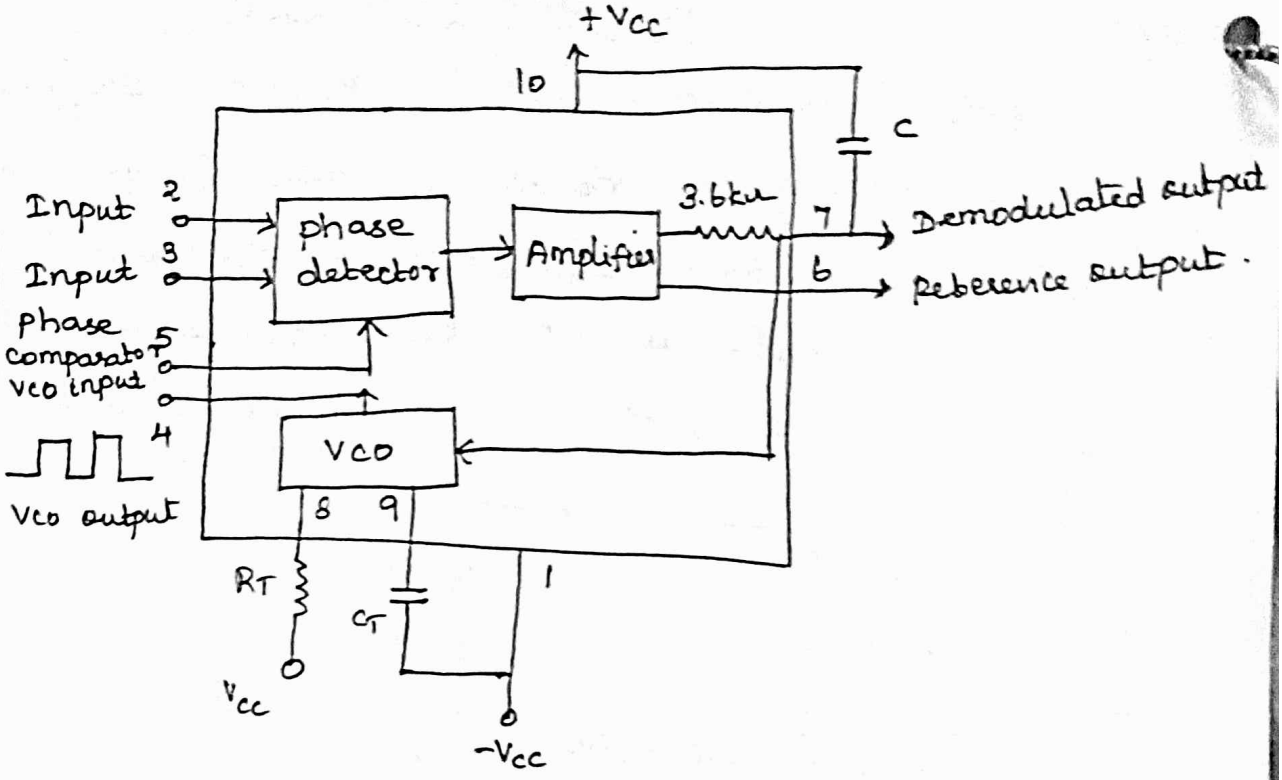
$$f_o = \frac{0.25}{R_T C_T} \text{ Hz}.$$

R_T, C_T → External resistor and capacitor connected to pin 8 & 9.

R_T ⇒ 2 kΩ - 20 kΩ is recommended.

⇒ A short circuit between pins 4 & 5 connects the VCO output to the phase comparator so as to compare f_o with f_s.

⇒ A capacitor C is connected between pin 7 & 10 to make a low pass filter with internal resistance of 3.6 kΩ.



NE/SE 565 PLL diagram :

Electrical parameters of 565 PLL are :-

Operating frequency range : 0.001 Hz to 500 KHz.

Operating voltage range : ±6V to ±12V.

Input level : 10mV rms min to 3Vpp max

Input Impedance : 10 kΩ

Triangle wave amplitude : 2.4 Vpp at ±6V supply voltage.

Square wave amplitude : 5.4 Vpp at ±6V "

Bandwidth adjustment range : < ±1 to ±60 %.

Derivation of Lock-in Range :-

If ϕ radians is the phase difference between the signal and the VCO voltage, then the output voltage of the analog phase dector is

$$V_e = K_\phi (\phi - \pi/2). \quad \text{—— (1)}$$

K_ϕ → phase angle to voltage transfer coefficient of the phase detector.

The control voltage to VCO is,

$$V_c = A K_\phi (\phi - \pi/2). \quad \text{——— (2)}$$

A → voltage gain of the amplifier. This V_c shifts VCO frequency & from its (f_0) to a (f) is given by,

$$f = f_0 + K_v V_c. \quad \text{——— (3)}$$

K_v → voltage to frequency transfer co-efficient of the VCO

when PLL is locked in to signal frequency f_s, then

$$f = f_s = f_0 + K_v \cdot V_c. \quad \text{——— (4)}$$

$$V_c = (f_s - f_0) K_v = A K_\phi (\phi - \pi/2). \quad \text{——— (5)}$$

$$\phi = \pi/2 + \frac{(f_s - f_0) K_v}{A K_\phi} \quad \text{——— (6)}$$

$$V_{c(max)} = \pm (\pi/2) K_\phi A. \quad \text{——— (7)}$$

The maximum VCO frequency swing that can be obtained is given by,

$$\text{from (5)} \Rightarrow (f - f_0)_{max} = K_v V_{c(max)} = K_v K_\phi A (\pi/2) \quad \text{——— (8)}$$

$$f_s = f_0 \pm (f - f_0)_{max} \Rightarrow \text{from eqn (4)}$$

$$\text{from (8)} \Rightarrow \therefore f_0 \pm K_v K_\phi (\pi/2) A = f_0 \pm \Delta f_L \quad \text{——— (9)}$$

$2\Delta f_L$ → lock in frequency range

$$\text{Lock in range} = 2\Delta f_L = K_v K_\phi A \pi.$$

$$\Delta f_L = \pm K_v K_\phi A (\pi/2). \quad \text{——— (10)}.$$

$K_V = \frac{\delta f_0}{V}$ (from VCO, K_V value). (11) eqn.

$V = +V_{CC} - (-V_{CC})$.

$K_\phi = \frac{1.4}{\pi}$

$A = 1.4$.

Lock in range from eqn (10) becomes

$$\Delta f_L = \pm 7.8 \frac{f_0}{V} \quad \text{—— (11).}$$

Derivation of capture Range :-

When PLL is not initially locked to the signal, the frequency of the VCO will be its free running frequency f_0. The phase angle difference between the input signal and the VCO output voltage will be,

$$\phi = (\omega_i t + \theta_i) - (\omega_0 t + \theta_0)$$

$$= (\omega_i - \omega_0)t + \Delta\theta \quad \text{—— (1)}.$$

$$\frac{d\phi}{dt} = \omega_i - \omega_0 \quad \text{—— (2)}.$$

LPF is a simple RC network having the transfer function

$$T(f) = \frac{1}{1 + j(f/f_1)} \quad \text{—— (3)}$$

$$\Delta f = f_i - f_0.$$

$\Delta f > 3f_1$, LPF transfer function will be approximately,

$$T(\Delta f) = \frac{f_1}{\Delta f} = \frac{f_1}{(f_i - f_0)} \quad \text{—— (4)}.$$

The voltage V_c to drive the VCO is,

$$V_c = V_e \times T(f) \times A \quad \text{—— (5)}.$$

$$V_{c(max)} = V_{e(max)} \times T(f) \times A.$$

Capture range

$$\Delta f_c = \pm \left[\frac{\Delta f_L}{(8\pi)(3.6)(10^3)C} \right]^{1/2}.$$