PIE Tech

POLLACHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Approved by **AICTE** and Affiliated to **Anna University**)

sky is the limit

Department of Electronics and Communication Engineering

Regulation 2021

III Year – V Semester

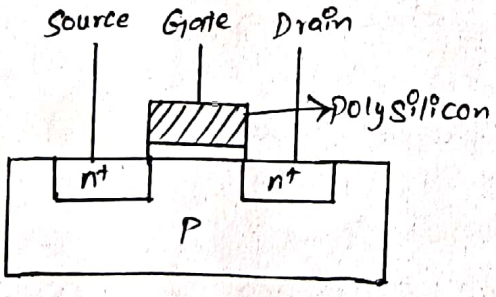
EC3552- VLSI and Chip Design

UNIT - I

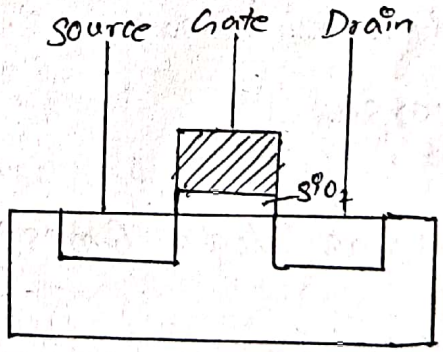
MOS TRANSISTOR PRINCIPLES

Introduction to MOS Transistor:

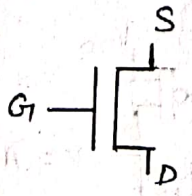
- A Metal-oxide-Semiconductor (MOS) transistor is formed by superimposing multiple layers of conducting and insulating materials like a sandwich-like structure.
- The 2 types of transistors - nMOS & PMOS.
- CMOS (complementary MOS) is a technology used in manufacturing of IC and processors. CMOS combines both nMOS & Pmos on a single chip.



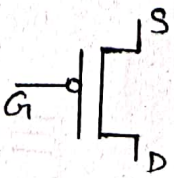
nmos



PMOS



nmos



PMOS

- The MOSFETs are simply called as FETs.

- The n^+ and p^+ regions indicate heavily doped n or P type silicon.

- Each transistor consists of a stack of conducting gate, insulating SiO_2 layer (glass), & substrate or body.

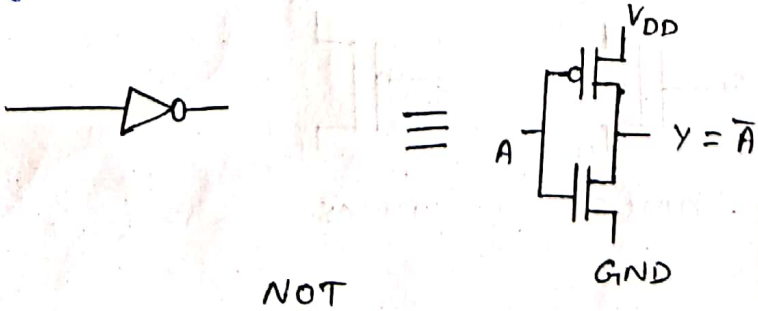
MOS as switch:

- The gate terminal acts as a control input as it can affect the electrical current between source and drain.

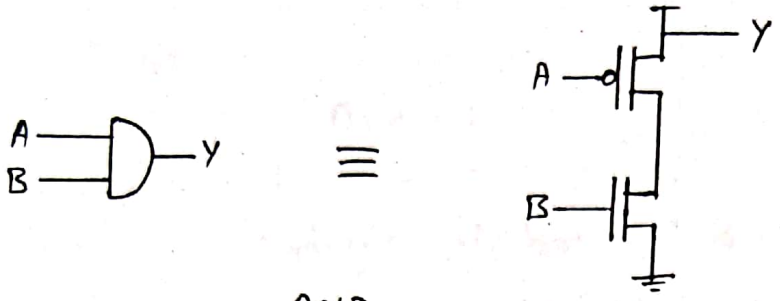
- So MOS transistors can be used as ON/off switches. When gate of nMOS is '1', transistor is ON, & vice-versa.

CMOS as Logic Gates:

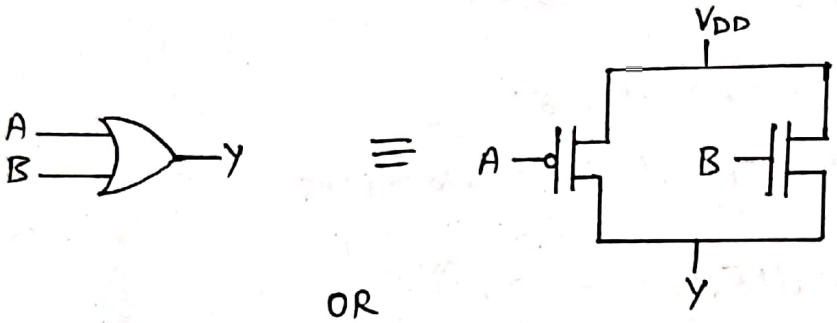
By using the switching property of MOSFET, basic logic gates function can be acheived using CMOS.



NOT



AND



OR

- Other than this, the CMOS is also used to realize the complex logic gates and 3 input gates.

Ideal I-V characteristics:

- The MOS transistors are voltage controlled devices. i.e., A voltage on gate terminal induces a charge between source and drain.

- The charge is dependent on V_{GS}. The current I_{DS} is dependent on both V_{GS} and V_{DS}. Their relationship can be explained using the derivation.

$$I_{DS} = \frac{Q_C}{\tau} \longrightarrow (1)$$

Q_C - Charge induced in channel

τ - electron transit time

$$\tau_{sd} = \frac{L}{V} \longrightarrow (2)$$

L - Length of channel

V - velocity of holes/electrons

$$V = \mu E_{ds} \longrightarrow (3)$$

μ - electron/hole mobility

E_{ds} - Electric field between source-Drain.

$$E_{ds} = \frac{V_{DS}}{L} \longrightarrow (4)$$

$$V = \mu \cdot \frac{V_{DS}}{L} \longrightarrow (5)$$

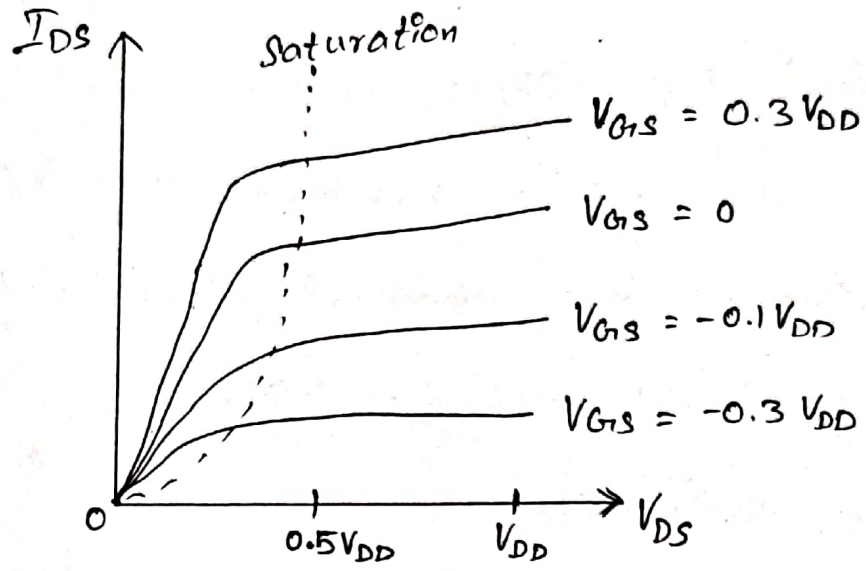
Sub (5) in (2).

$$\tau_{sd} = \frac{L^2}{\mu V_{DS}}$$

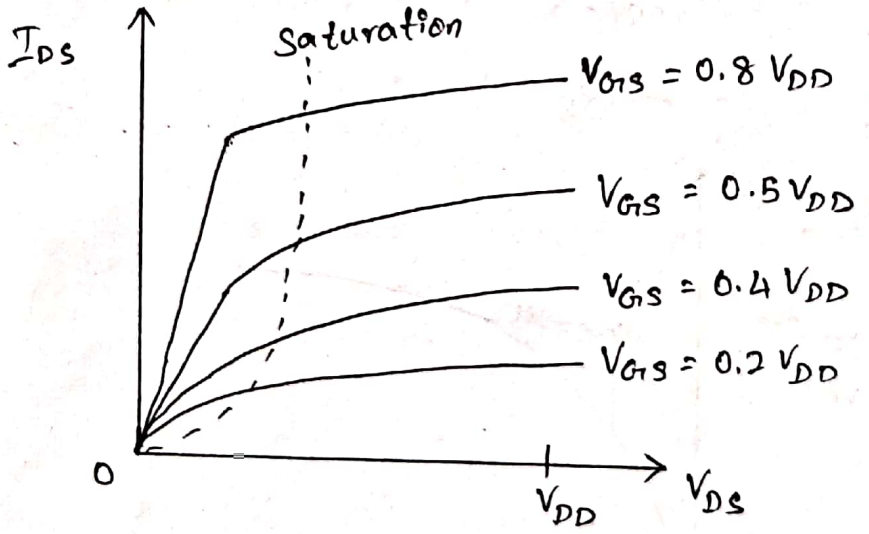
- The mobility of electrons & holes at room temperature is

$$\mu_n = 650 \text{ cm}^2/\text{V}$$

$$\mu_p = 240 \text{ cm}^2/\text{V}$$



Depletion mode



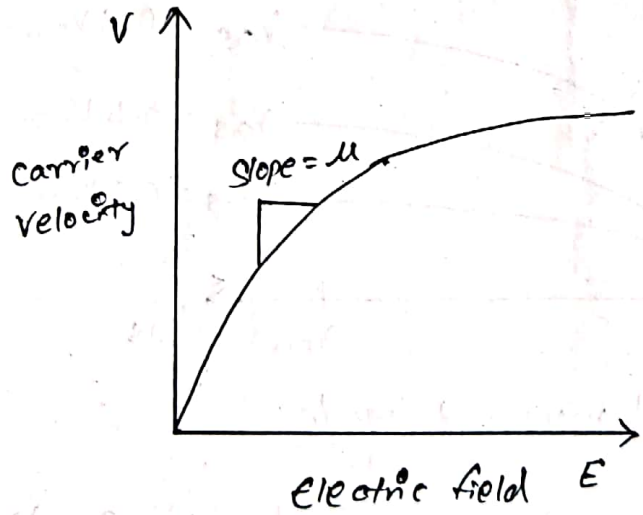
Enhancement mode

Ideally, the above characteristics are to be obtained. But it is impossible to realise these using the practical enhancement and depletion MOSFETs.

Non-Ideal I-V effects:

The various non-ideal I-V effects that can influence the electrical characteristics are:

1. Channel length Modulation
2. Body effect
3. Drain-induced barrier lowering
4. Subthreshold conduction
5. Gate oxide tunneling



Channel length Modulation:

As the voltage across MOSFET increases, the channel length can effectively shorten due to electric field at drain end of channel.

This effect leads to an increase in drain current.

Body Effect:

The body effect, also known as back-gate effect arises from influence of voltage applied to MOSFET's substrate or body terminal. This effect can lead to threshold variations.

Drain Induced Barrier lowering:

It is a phenomenon that occurs in MOSFET as the channel length of transistor decreases. It refers to the reduction of effective energy barrier at Source-Drain region under influence of drain voltage.

Sub-Threshold Conduction:

When the voltage applied to gate is below threshold voltage, the channel is not fully formed & only small leakage current called sub threshold leakage current flows between source-Drain terminals.

Gate oxide tuneling:

It is a process where electrons/holes tunnel through the oxide layer, allowing the charge carriers to flow between the gate and channel. The two mechanisms of tuneling are:

- Direct tuneling
- Fowler-Nordheim tuneling.

Drain Punch-through:

When a high voltage is applied to drain, the depletion region around drain may extend to source, causing the current to flow irrespective of gate voltage is called as drain puch-through.

It occurs due to.

1. Higher voltage to gate
2. Arcing across the thin oxide.

MOSFET Characteristics under Static & Dynamic Conditions:

The various static and dynamic characteristics of MOSFET are listed below:

Static characteristics:

1. Threshold voltage (V_{th})
2. Drain - source on resistance (R_{DS})
3. Drain current (I_D)
4. Output characteristics (I_D vs V_{DS})
5. Transfer characteristics (I_D vs V_{GS})

1. Threshold voltage:

The minimum gate to source voltage required to establish a conducting channel between the source and drain terminals. It determines the on/off state of MOSFET.

2. Drain Source on resistance:

The resistance between the drain and source terminals when the MOSFET is in on-state. It

affects the power dissipation and efficiency of the device.

3. Drain current:

The current flowing from the drain to the source terminal under a given gate to source voltage (V_{GS}) and drain to source voltage (V_{DS}).

It depends on the applied voltages and the characteristics of MOSFET.

4. Output characteristics:

The plot of I_D vs V_{DS} at a constant V_{GS} is called as output characteristics. It shows the region of operation, such as the saturation region and triode region.

5. Transfer characteristics:

The plot of drain current versus gate to source voltage at a constant V_{GS} is called as transfer characteristics. It indicates the threshold

voltage, MOSFET's behaviour on ON/OFF states and the device's transconductance.

Dynamic characteristics:

The dynamic characteristics of a MOSFET are:

1. Gate capacitance
2. Switching time
3. Output capacitance
4. Miller effect

1. Gate Capacitance:

The capacitances between gate-source and gate-drain is called as Gate capacitance (C_{GS} & C_{GD})

They play a crucial role in charging & discharging of the gate voltage, & speed of MOSFET.

2. Switching time:

It refers to the time required for the MOSFET to transition between the ON & OFF states. It depends on gate capacitance, gate resistance & load.

3. Output Capacitance:

The capacitance between the drain and the source terminals when the MOSFET is in off state is called output capacitance.

It affects the transient response and energy losses during switching.

4. Miller Effect:

It refers to the increase in effective gate capacitance due to the voltage amplification between the input and output terminals of MOSFET.

It affects the switching speed & can lead to oscillations.

Noise Margin:

Noise margin is the allowable input gate voltage so that the output will not be corrupted.

Technology Scaling :

It refers to the process of reducing the size of electronic devices and components, such as transistors, IC and other semiconductor devices.

Technology scaling is often associated with Moore's law, which states that the number of transistors on a chip doubles approximately every two years.

Scaling down the size of transistors & other components leads to improved device performance. Smaller transistors can switch faster, resulting in higher operating frequencies.

As the size of transistor shrinks, it requires lesser power to switch between ON/OFF states.

The VLSI Technology scaling is aimed at acheiving the smaller line widths and size for higher packing density.

Merits of Scaling:

1. Scaling allows integration of more components on the same chip area.
2. Improved switching performance
3. Shorter signal propagation delays.
4. Enhanced circuit performance
5. Reduced power consumption
6. Cost reduction in manufacturing of the semiconductor devices.
7. Ability to integrate more functionality on a single chip.
8. Leads to new device architectures, novel materials and advanced manufacturing techniques.
9. Lesser leakage currents and lesser manufacturing complexities.

Demerits:

1. Even though overall power consumption reduces, power consumption per unit area increases.

2. Device gets heated up during operation.

3. Carrier mobility reduces which inturn reduces gain of the device.

4. Reduced conductor size decreases the current carrying capacity.

5. To reduce heat generated, forced cooling is required.

Lambda based Design Rule:

It is a methodology used in semiconductor manufacturing to establish a scalable measurement unit and spacing requirements.

The Lambda (λ) represents a reference length or pitch, which is typically chosen based on the process technology node or the minimum feature size of the semiconductor process.

This method simplifies the design process by expressing dimensions, spacing and other layout in terms of λ.

The few aspects of Lambda based design rule are:

Lambda Definition:

Lambda represents a fixed reference length or pitch. It is derived based on the process technology node or minimum feature size.

For example, if minimum feature size is 50nm, one lambda might be defined as 50nm.

Dimensions and Spacing:

Instead of specifying a metal wire width as 0.25 μm, it is expressed as 5λ (assuming 1λ = 50nm).

Similarly, spacing between two adjacent features might be defined as 3λ.

In General, it is to be noted that the value of λ varies for each device and designers can fix the value to their convenience.

Modes of scaling:

1. Lithography scaling
2. Transistor scaling
3. Interconnect scaling
4. Material innovations
5. 3D integration

Scaling factors for device parameters:

1. Length & width scaling factor.
2. Voltage scaling factor
3. Current scaling factor
4. Performance scaling factor.

Gate Capacitance:

The gate capacitance refers to the capacitance associated with the gate terminal of MOSFET. It consists of 2 components - C_{GS} & C_{GD}.

Parasitic Capacitance:

The parasitic capacitance of MOSFET refers to the capacitance that exist between various terminals and regions of the device.

These parasitic capacitances have an impact on the device's performance and can affect its high frequency behaviour.

The components of gate capacitance are C_{GS}, C_{GD}, C_{GB} and C_{DS}.

Power Consumption:

The Static CMOS gates are very power efficient. They dissipate nearly zero power while idle.

The power dissipation in a CMOS is,

$$P = V_{DD} \cdot I_{DC}$$

Where,

V_{DD} - Power supply voltage

I_{DC} - Current drawn from power supply.

The CMOS power dissipation is categorized into two types:

- Static power dissipation
- Dynamic power dissipation.

Static power Dissipation:

It refers to the power consumed by a device when it is in a static or idle state, regardless of any active signals being processed.

It arises from the leakage currents that flow through transistors and other components.

The major causes of static power dissipation are:

1. Subthreshold conduction through off transistors
2. Tunneling current through gate oxide
3. Leakage current through reverse biased diodes

The static power dissipation is given as:

$$P_{static} = I_{static} \cdot V_{DD}.$$

The static power dissipation is due to leakage current flowing through the reverse biased junctions of transistors.

The leakage current per unit drain area ranges between 10 to 100 pA/um². The total static power dissipation is given as:

$$P_{Total\ static} = \sum_{1}^{n} I_{static} \cdot V_{DD}$$

Dynamic Power Dissipation:

The dynamic power dissipation refers to the power consumed by a device during its active operation, specifically during the switching of signals and the charging and discharging of internal capacitances.

It is given by the equation,

$$P_{dynamic} = 0.5 \times C_L \times V^2 \times f$$

Where,

$P_{dynamic}$ - Dynamic power dissipation

C_L - Load Capacitance

V - Supply voltage

f - frequency of signal transitions.

The various factors that contribute to the dynamic power dissipation are:

1. Capacitive charging / discharging
2. Clock power
3. Short-circuit power
4. Activity factor

Reducing the dynamic power dissipation is crucial for improving the energy efficiency. The various techniques employed to minimize dynamic power are:

1. Clock gating
2. Voltage scaling
3. Low power circuit design.

Short circuit power Dissipation:

It indicates the power dissipation due to short circuited current in an unloaded inverter. The S.C power dissipation is given as,

$$P_{sc} = \frac{K}{12}(V_{DD} - V_t)\frac{3t_{rf}}{t_p}$$

Where,

t_p - period of i/p waveform

t_{rf} - Rise time of i/p waveform

K - Constant.

Need to estimate power dissipation:

The power dissipation affects

1. Performance
2. Reliability
3. Packaging
4. Cost
5. Portability.

factors influencing CMOS power Consumption

There are 3 major sources of power dissipation,

$$P_{avg} = P_{switching} + P_{s.c} + P_{leakage}$$

Techniques to reduce power consumption:

The following techniques can be used to reduce the power consumption,

1. Reduce voltage
2. Reduce switching activity
3. Reduce physical capacitance
4. Ordering of input signals
5. Minimizing glitching activity
6. Minimizing number of operations.

Low Power Optimization:

The low power optimization technique of MOSFET is aimed at reducing the power consumption

Some of the commonly used techniques for low power optimazation are:

1. Threshold voltage Adjustment:

By adjusting the threshold voltage of MOSFET, the power consumption can be lowered. Lowering the threshold voltage reduces the leakage currents and static power dissipation.

2. Scaling down supply voltage:

Reducing the supply voltage of MOSFET lowers the power consumption.

3. Subthreshold operation:

Operating the MOSFET like V_{GS} below the threshold voltage can reduce the power consumption significantly.

4. Multi-V_t Techniques:

Using multiple threshold voltage transistors

in a single circuit allows better power optimi-
-zation.

5. Power Gating:

Power gating involves selectively turning off the power supply to specific blocks or components of the circuit when they are not in use.

6. Clock gating:

The clock signals are selectively enabled or disable based on the activity of circuit blocks.

All the above mentioned techniques can be applied individually or in combination depending on the specific requirements of the application.

UNIT - 2

COMBINATIONAL LOGIC CIRCUITS

Introduction:

The combinational logic circuits are the digital circuits that perform a specific logic operation based on the current input values.

The output of a combinational logic circuit depends only on the present input values and not on any previous inputs.

Propagation Delay:

Propagation delay refers to the time it takes for a signal to travel through a circuit or a component from its input to its output.

It is a measure of the time delay experienced by a signal as it propagates through the circuitry.

In CMOS logic circuits, the propagation delay is mainly due to critical paths. It is nothing but the logic paths through the CMOS circuit.

The delay estimation can be done through:

1. Rise time:

The time required for a waveform to rise from 20% to 80% of its steady state value. It is denoted as 't_r'.

2. fall time:

It is the time required for a waveform to fall from 80%. to 20% of its steady state value. It is denoted as t_f.

3. Edge Rate:

Edge rate is the average of rise time and fall time. It is denoted as t_{rf}.

$$t_{rf} = \frac{t_r + t_f}{2}$$

Propagation Delay time:

It is the maximum time from the input crossing 50%. to the output crossing 50%. It is denoted by 'tpd.'

Contamination Delay time:

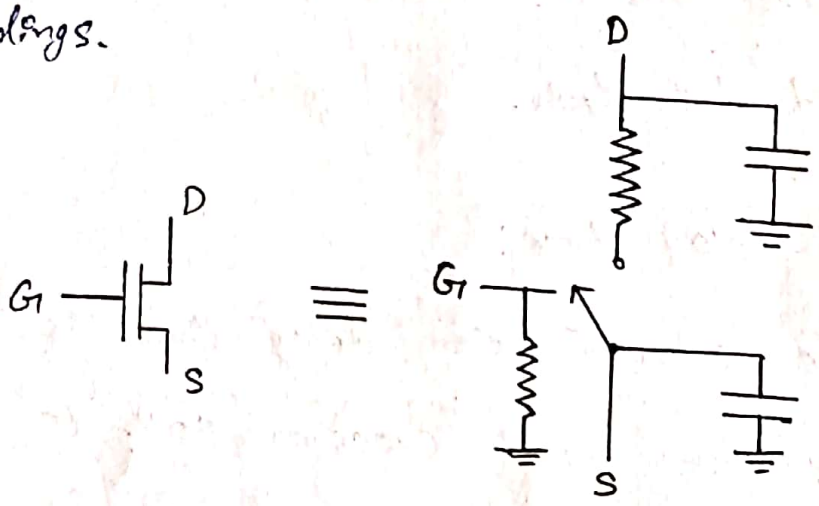
The contamination delay time is the minimum time from input crossing 50%. to the output crossing 50%..

RC Delay Model:

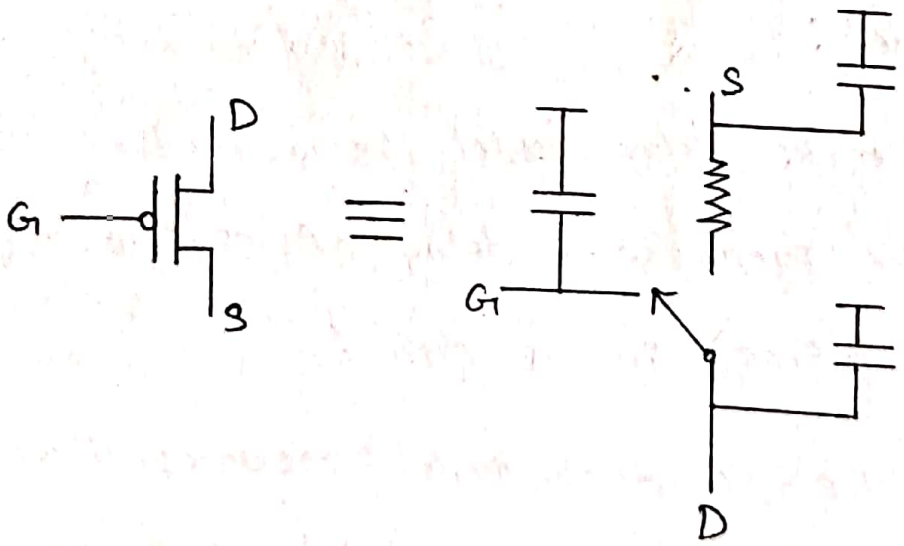
The RC delay model is a method used to estimate the propagation delay of signals through interconnects (wires) in a circuit.

The RC delay model assumes that the interconnect can be represented as a RC network, where the resistance represents the resistance of

the wire and the capacitance represents the inherent capacitance between the wires and its surroundings.



N-MOS



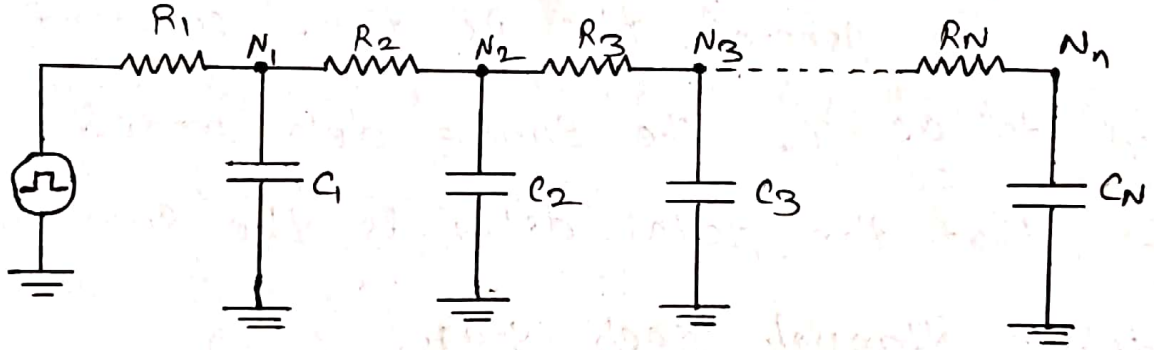
P-MOS

When multiple transistors are in series, the equivalent resistance is the sum of each

individual resistance. When multiple transistors are in parallel, the equivalent resistance is lower.

The RC delay model is often used in conjunction with other models, such as Elmore delay model to estimate the overall delay of the signal path in a circuit.

Elmore Delay Model:



The Elmore delay model is a widely used method for estimating the signal propagation delay in electronic circuits, particularly RC networks.

It provides a simple and efficient way to estimate the delay based on the RC time constant.

In the Elmore delay model, the delay is calculated as the sum of the products of resistance values and capacitance values along the signal path.

The model assumes that the signal propagates as a series of charging and discharging RC stages.

In general, the RC time constant is referred to as τ. The Elmore delay model considers that the total delay is the sum of the delays through each stage.

The disadvantage of Elmore delay model is that, it assumes all the capacitances are charged and discharged simultaneously.

Also, it assumes that the interconnects are purely resistive, disregarding inductance effect.

Parasitic Delay:

The parasitic delay refers to the additional delay introduced in an electronic circuits due to parasitic elements present in the circuit.

The parasitic elements includes parasitic capacitance, parasitic resistance & inductance. The delay of gate when it drives zero load is parasitic delay.

Logical Effort Model & Effort Delay:

The logical effort model is a design methodology used to optimize the performance of digital circuits.

The effort delay refers to the delay associated with driving a load in digital circuits.

The logical effort is a measure of the relative sizing of the gate compared to a reference gate.

The Logical effort is also defined as the ratio of Input capacitance of the gate to the Input capacitance of an Inverter which delivers the same output current.

Stick Diagram:

A stick diagram is a graphical representation used in Ic design to illustrate the layout of a circuit using simple shapes and lines.

The main purpose of the stick diagram is to provide a visual representation of the circuit layout that can be used to analyse and optimize the circuit for performance, area and other design considerations.

The stick diagrams are useful in early understanding of circuit design rather than doing detailed layout implementation.

In recent days, the stick diagrams have became less prevalent as moder Ic design practices such as advanced CAD tools are used for more accurate and detailed representations.

However, the stick diagrams still serves as a valuable tool and aid in understanding the fundamental principles of Ic layout design.

The stick diagrams are used to convey the layer information through the use of colour code.

Colour codes:

Green - for n diffusion & other thin oxide regions.

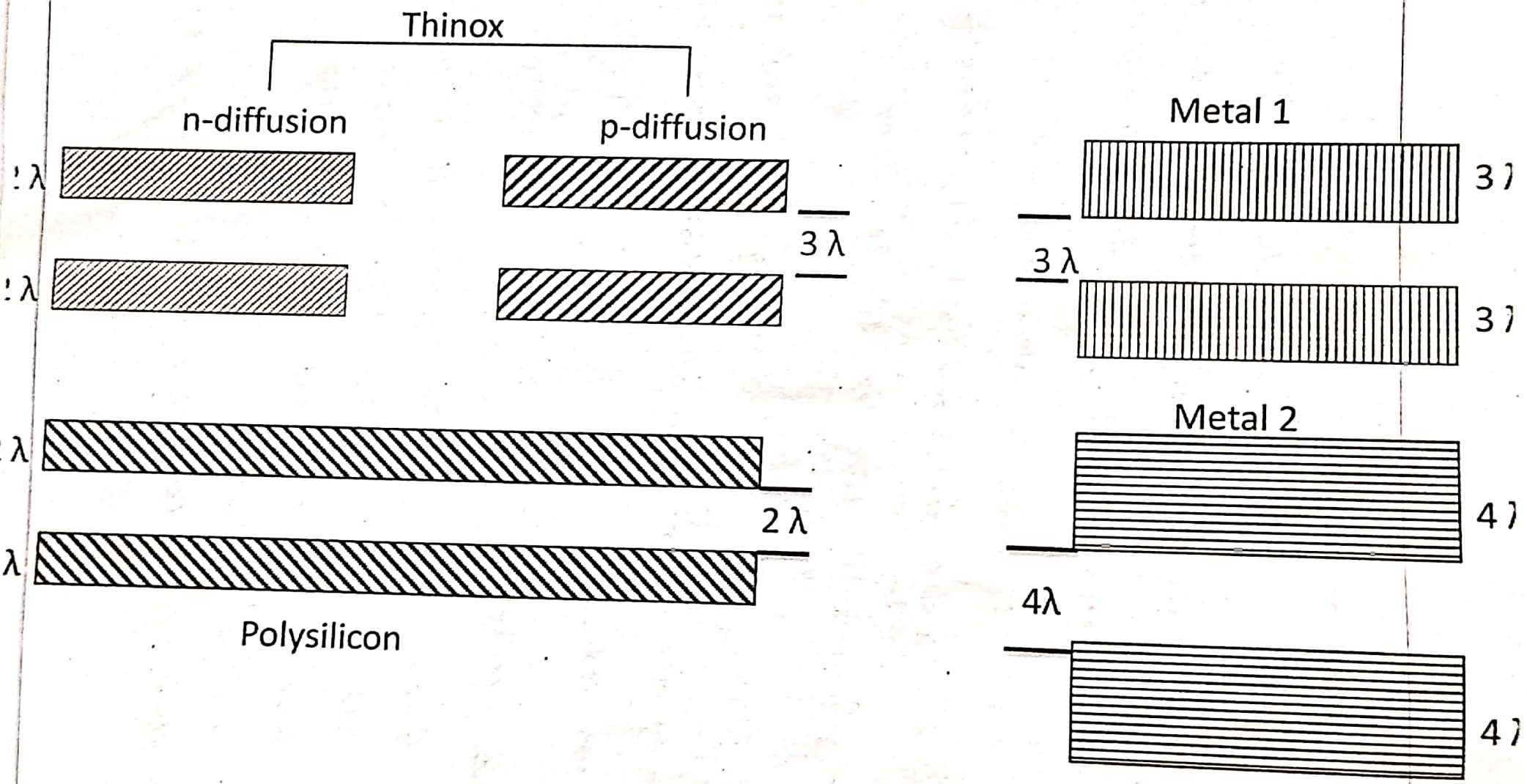
Red - Only 1 polysilicon layer is involved.

Blue - only one metal layer is involved.

Yellow - Implant

Black, Brown - Contacts.

DESIGN RULES

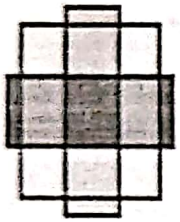


Transistor

Metal-Polysilicon

Polysilicon

Diffusion



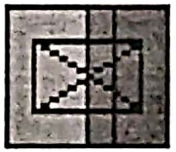
Depletion Transistor

Metal-Diffusion

Metal

Contact

Polysilicon Pin



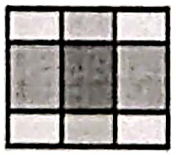
Butting

Implant

Diffusion Pin

Overglass

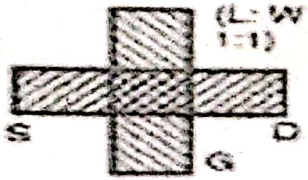
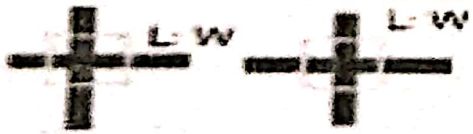
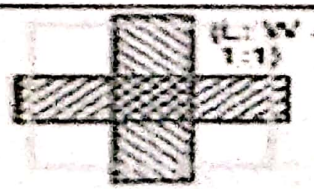
Metal Pin



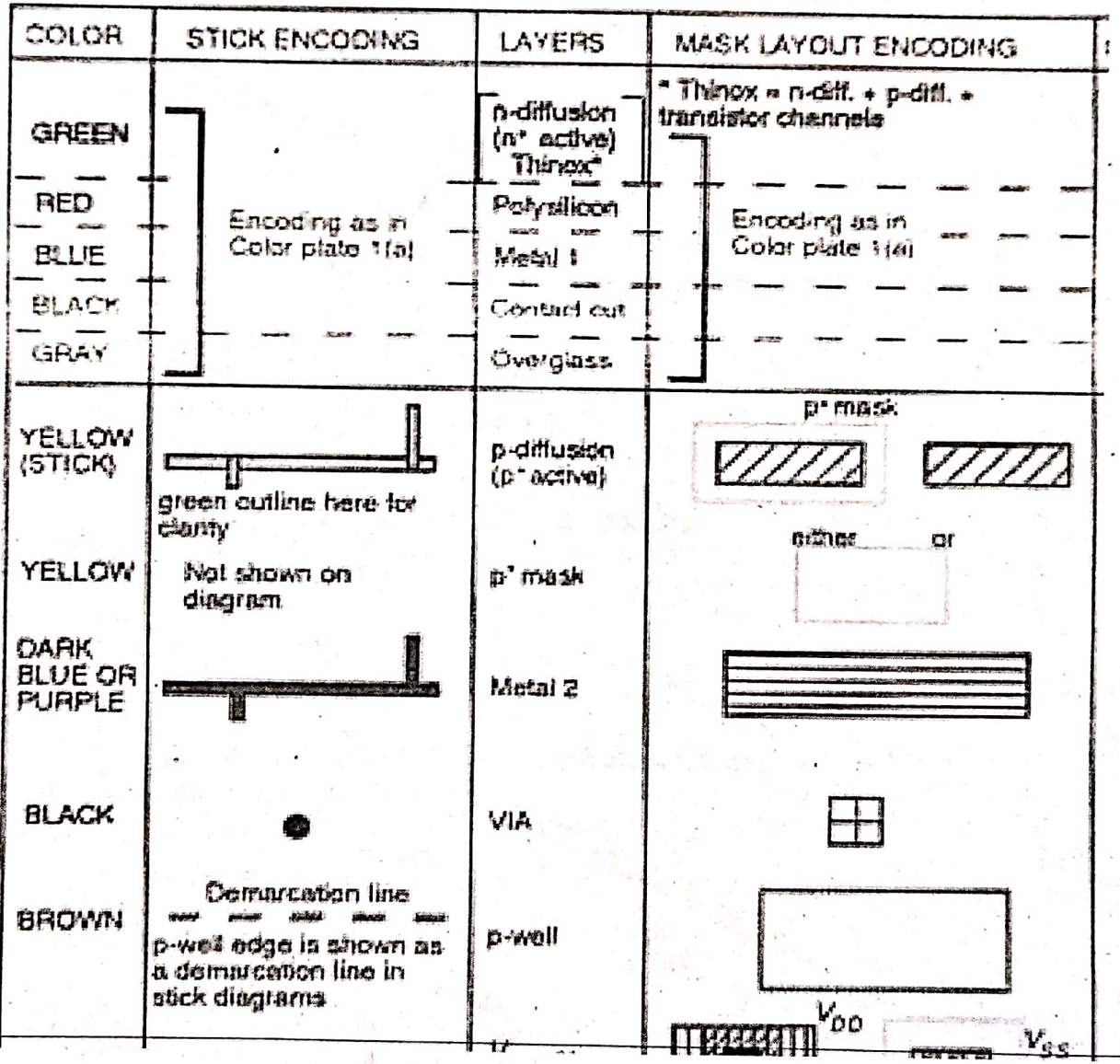
Buried

Buried

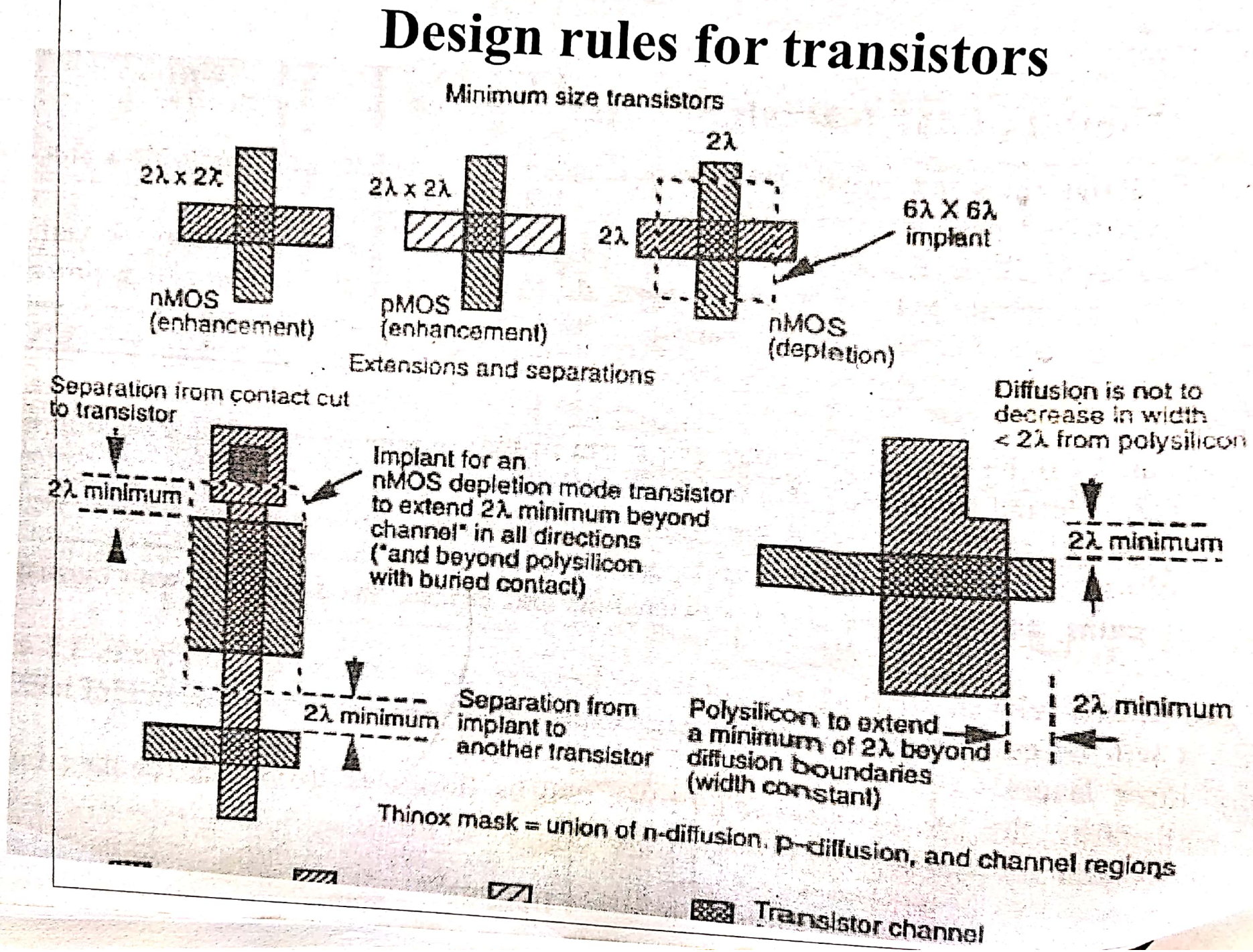
COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN		n-diffusion (n+ active) Thinox*	 *Thinox = n-diff. + transistor channels	ND
RED		Polysilicon		NP
BLUE		Metal 1		NM
BLACK		Contact cut		NC
GRAY	NOT APPLICABLE	Overglass		NG
nMOS ONLY YELLOW		Implant		NI
nMOS ONLY BROWN		Buried contact		NB

FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
n-type enhancement mode transistor			
Transistor length to width ratio L: W should be shown.			
n-type depletion mode transistor nMOS only			
Source, drain and gate labelling will not normally be shown.			

Encodings for CMOS process



Design rules for transistors



Layout Diagrams :

The Layout diagrams are used in IC design to illustrate the detailed arrangement and placement of circuit components on a chip.

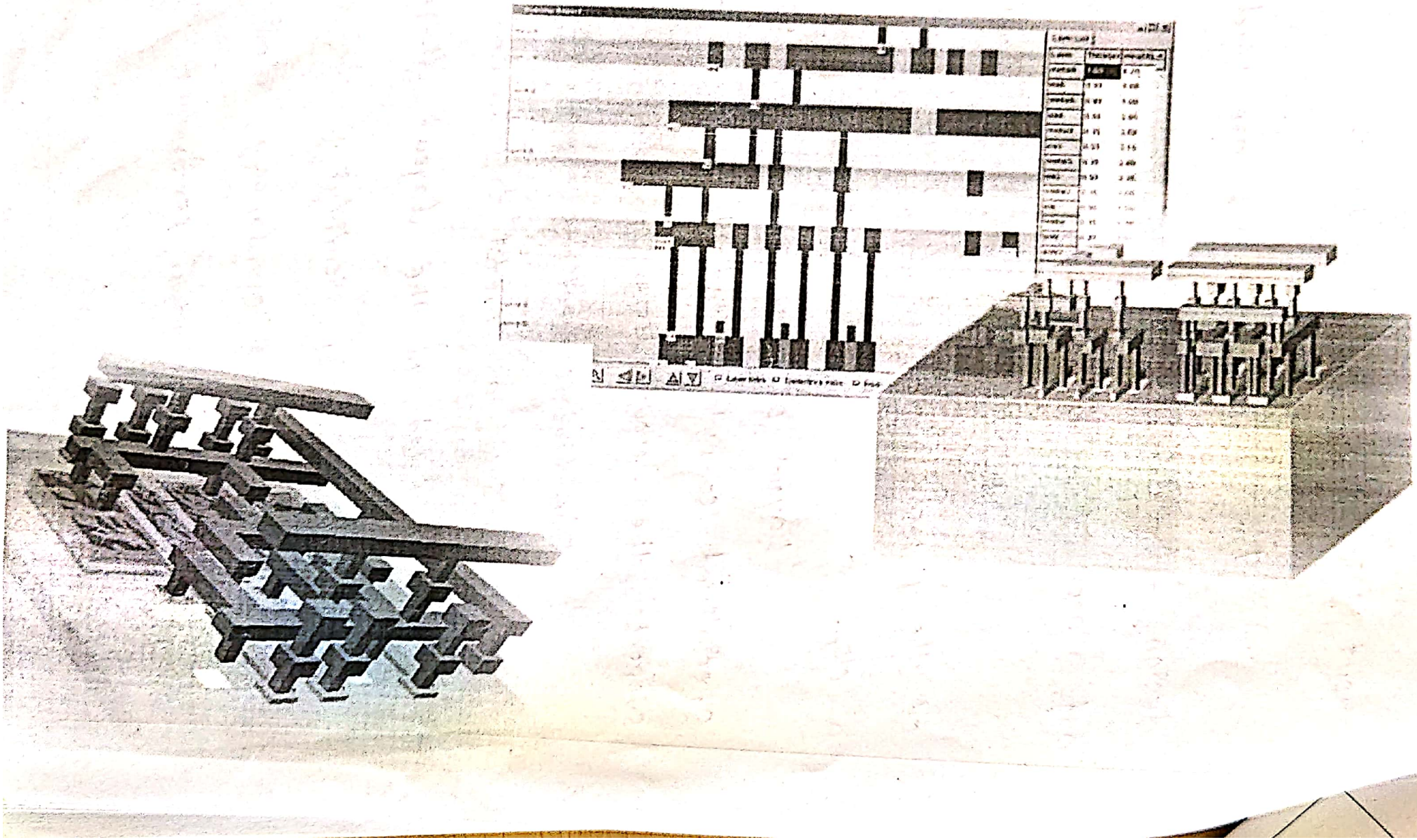
These diagrams provide a visual representation of the physical layout of the circuit components on a chip.

Layout diagrams are created using the specialized computer-aided design (CAD) tools that supports the layout design process.

The interconnections between the components such as metal traces and contacts are also included in the layout diagram.

They help in identifying the potential design issues such as overlapping, spacing violations etc., It also ensures power, performance & area requirements.

The 3-D View of a Design



There are number of approaches to describe the design rules. They are:

1. Micron design rule
2. Lambda design rule

Micron Design rule:

The micron design rules are given as a list of minimum feature sizes and spacings for all the marks required in the given process.

Lambda Based Design Rule:

The λ refers to a unit of length that is equal to the minimum feature size of the process technology being used.

This method simplifies the specification of design rules by expressing them in terms of lambda rather than using absolute values.

Contact cuts:

The contact cuts provide the electrical connections between different layers of IC, and allows the signals to pass vertically from one layer to another.

The 3 possible approaches for establishing contacts between polysilicon and diffusion in nMOS circuits are:

1. Poly to metal & metal to diffusion
2. A buried contact - poly to diffusion
3. A butting contact - poly to diffusion using metal.

Static Logic Gates:

The static logic gates uses only static CMOS technology. It is widely used in modern IC technology because of their low power consumption.

The 2 most commonly used types of static logic gates are:

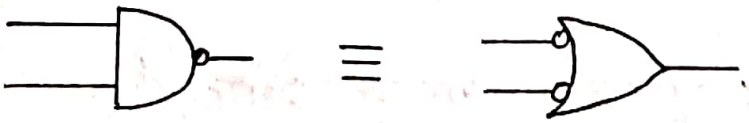
1. Static CMOS NAND gate
2. Static CMOS NOR gate

Bubble Pushing:

Bubble pushing is a technique used in digital circuit to optimize gates and to reduce the propagation delay.

The term bubble refers to the logical inversion of a signal represented by NOT gate.

De-Morgan's law



NAND ≡ Inverted OR

$$\overline{A.B} = \bar{A} + \bar{B}$$

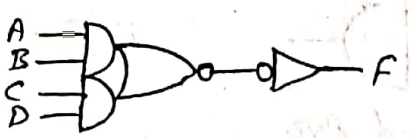
NOR ≡ Inverted AND

$$\overline{A+B} = \bar{A}.\bar{B}$$

The main goal of bubble pushing is to reduce the complexity of circuit by introducing additional bubbles in the path & reducing the number of logic levels or stages that the signal needs to pass through which ultimately reduces the delay.

Compound Gates:

The compound gates are the logic gates that can perform more than a single basic logic operation. They are constructed by combining multiple basic logic gates in a specific configuration to implement a more complex logic function.



AOI.

Dynamic Logic Gates: vs Static Logic Gates:

S.No	Aspect	Static	Dynamic
1.	Operation	Output is directly connected to input without any storage elements.	Has storage elements to store logic states temporarily (like capacitor)
2.	Power Consumption	Power efficient	Requires more power.
3.	Speed.	Lower propagation delay.	Higher propagation delay.
4	Area	Requires more Silicon area.	Comparitively less.
5.	Complexity	Easy to design	Complex.

Ratioed Circuit:

The ratioed circuit uses a combination of parallel transistors to implement the basic logic gates.

The key feature of ratioed circuits is that it reduces the number of transistors required to implement a given logic function.

It also has a disadvantage of reduced robustness and increased power dissipation. It is used in current mirrors, differential amplifiers, ADC and DAC circuits.

Pass Transistor Logic:

The pass transistor Logic (PTL) is a type of Digital logic design used in IC for implementing the logic functions, which comes as an alternative for traditional Static CMOS.

In PTL, transistors are used as switches to allow or block the flow of signals which results in realization of different logic gates and circuits.

The basic building block of PTL is a pass transistor which is a type of MOSFET. The FET acts as a switch and allows the passage of input signal when it is activated. They dont need any intermediate gates like NAND or NOR.

There are 2 types of pass transistor configurations:

1. Transmission Gate (TG)
2. Pass Gate Logic (PGL)

Transmission Gate:

The transmission gate consists of a pmos and an nmos connected in parallel. The gates are controlled by complementary control signals. When control signals are active, the pass transistor behaves as a closed switch & vice versa.

Pass Gate Logic:

It is uses a single MOSFET as a pass transistor, & controlled by a single control signal. When control signal is high, pass transistor is ON & vice versa.

The following are the advantages of PTL:

1. Reduced transistor count
2. Lower power consumption
3. Higher speed
4.

Power Dissipation:

The power dissipation is the amount of energy consumed or lost by the circuit over a certain period of time.

Low power Design principles:

It is a set of guidelines and techniques used by IC designers to minimize the power

consumption in IC and electronic systems. Some of the key low power design principles are:

1. Clock gating
2. Power gating
3. Voltage gating
4. Sub-Threshold operation
5. Adaptive voltage scaling.
6. Sleep mode and power modes
7. Efficient memory design
8. Optimal transistor sizing

Taking care of the above mentioned principles will drastically reduce the power consumption of the IC circuits.

UNIT-3

SEQUENTIAL LOGIC CIRCUITS & CLOCKING STRATEGIES

Introduction:

The sequential logic circuits are a type of digital logic circuits in which the output not only depends on the current input but also on the previous stages of the circuit.

Hence, the sequential logic circuits needs the memory elements to store information and to use in future.

The fundamental building block of a sequential logic circuit is flip-flop, which is a bistable multivibrator capable of holding one of two stable states: 0 or 1. The commonly used flip-flops are SR ff, D ff, JK ff.

By combining the flip flops and logic gates (AND, OR, NOT, etc)., more complex sequential logic circuits such as counters, registers, are formed.

Static Latches and Registers:

The static latch is a simple storage element that can store one bit of data and retain it as long as power is supplied. It is composed of cross coupled NOR or NAND gates.

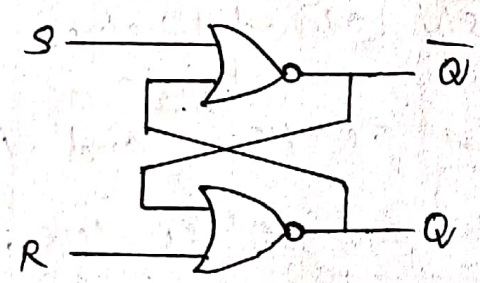
The two most common types of static latches are

1. SR latch
2. D Latch.

A static Register is a collection of flip flops connected togother to store multiple bits of dada simultaneously. The number of flip-flops determines its capacity.

SR flip-flops:

The SR flip-flops also known as set-Reset flip-flop. is a basic type of sequential logic circuit. It is a bistable multi-vibrator, meaning it has two stable states, & it can stay in one of these states until a control signal changes its state. The flip-flop has 2 inputs (S & R) and 2 output (Q & Q')



S	R	Q	Q'
0	0	Q	Q'
0	1	0	1
1	0	1	0
1	1	x	x

Truth table

The 'x' in the last row indicates undefined state, which should be avoided in practical implementations, because it leads to unpredictable behaviour.

Working:

1. When both inputs are low, the flip-flop remains in its current state and there is no change in the output. This is hold state and it maintains the previously stored value.

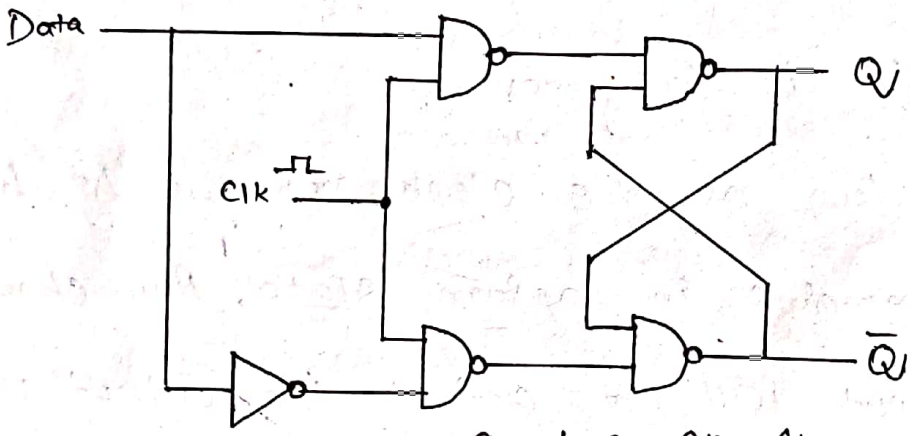
2. When S input is High and R is low, the output Q is high and Q' is low. This is set state, where the output is forced to 1.

3. When S is low and R is high, the outputs Q is low and Q' is High. This is reset state, where the output is forced to 0.

4. When both inputs are high, output is undefined state.

D flip-flop:

The D flip-flop, also known as the data or Delay flip-flop is a type of sequential logic circuit. It is a clocked storage element that stores one bit of data.



Gated SR flip-flop

clk	D	Q	Q'
0	X	Q	Q'
1	0	0	1
1	1	1	0

Truth table

Working:

1. When the clock input is low, the flip-flop is in a hold state. The output retains its current state, regardless of data input. Q' also held in its previous state.

2. When clock is 1, it enters capture state. At this moment, Q takes value of data input and Q' will be its reverse.

3. As long as the clock remains high, flip flop remains in capture state. Any change in data input will not affect the output until the next rising edge of the clock.

4. When clock goes low, the flip-flop goes to hold state, retaining the, Q and Q' at the last captured values.

Dynamic Latches and Registers:

A dynamic latch, also known as a clocked latch uses the concept of capacitor charging and discharging to store the data. It requires an external clock signal to control its operation.

The most common type of dynamic latch is the master-slave latch, which consists of 2 cascaded stages, master and slave.

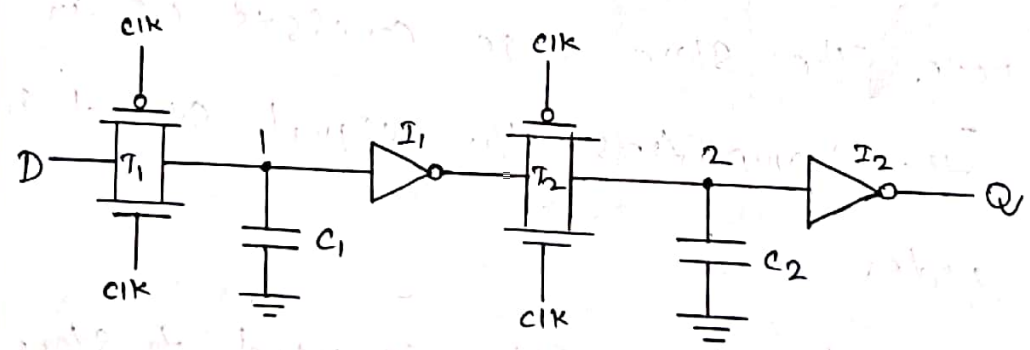
The Master stage consists of a transmission gate that connects the data input to internal node. The slave stage consists of an inverter that amplifies the signal stored in internal node.

A dynamic register is used to store multiple bits of data using a common clock signal. But they consume more power compared to static registers.

Dynamic Transmission-Gate Edge Triggered Register

A transmission gate is a type of switch implemented using CMOS. It acts as a pass gate, allowing signals to pass through when the gate is active and blocking them when it is inactive.

The primary advantage of dynamic transmission gate registers over static registers is that they require fewer transistors, which leads to reduced area and power consumption.



When the ~~input is~~ clock is zero, the input data is sampled on storage node 1, which has an equivalent capacitance of C, consisting

of gate capacitance of I_1, the junction capacitance of T_1 and the overlap gate capacitance of T_1.

During this period, the slave stage is in hold mode. On the rising edge of clock, T_2 turns ON and the value sampled on node 1 propagates to output Q, and node 2 stores the inverted version of node 1.

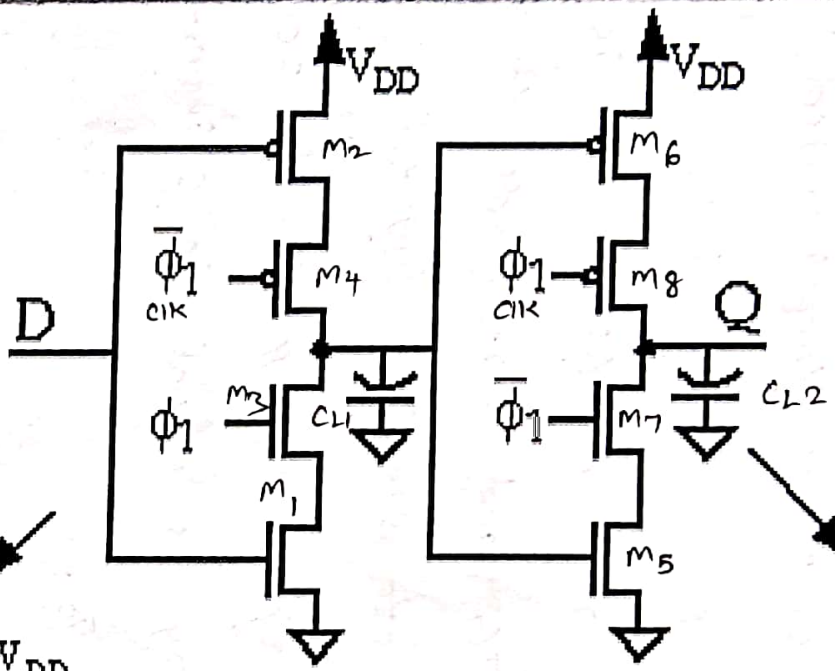
The set up time of this circuit is simply the delay of TG and corresponds to the time it takes node 1 to sample D input.

The hold time is approximately zero. The propagation delay is equal to 2 inverter delay plus delay of T_2.

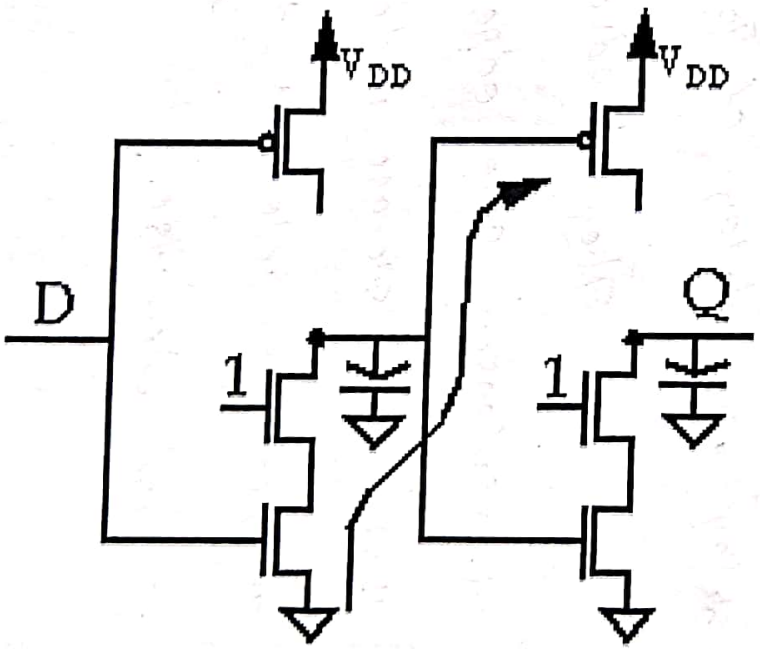
The disadvantage of dynamic transmission gate edge triggered registers is that the storage nodes has to be refreshed at periodic intervals to prevent loss due to charge leakage.

Clocked CMOS Register (CCMOS)

Consider the single phase case.



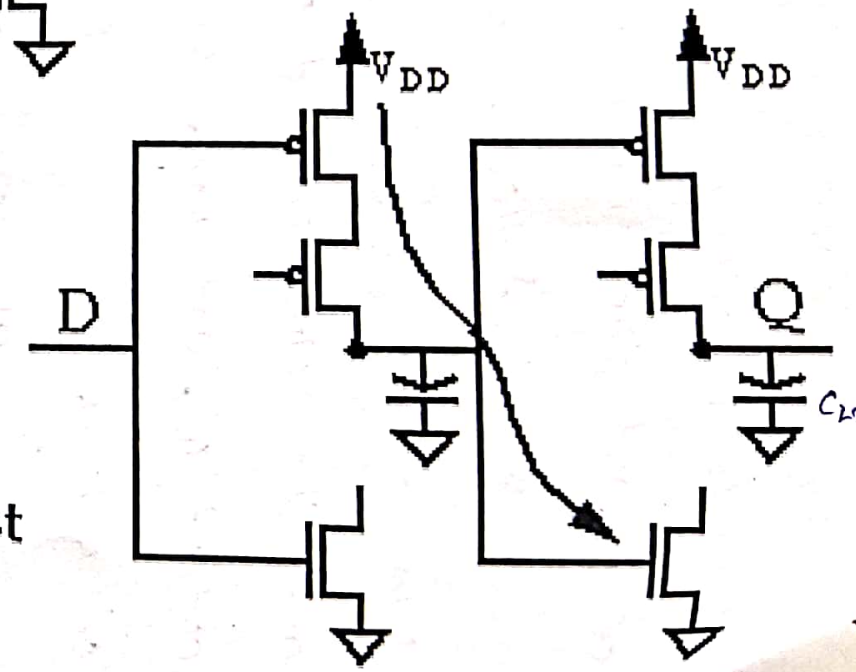
1-1 overlap.



No race is possible !

In order for D to race to the Q, a pull-up followed by a pull-down must be enabled.

0-0 overlap.



Clocked C-MOS Register:

When the clk = 0, the master stage acts as an inverter sampling the inverted version of D on the internal node x. The master stage is in the evaluation mode, meanwhile, the slave section is in a hold mode Both M_7 and M_8 are off, hence decoupling the output from input. The output Q retains its previous value stored in C_{L2}.

The roles are reversed when clk = 1. The master section is in hold mode (M_3 - M_4 - OFF) and the (M_7 - M_8 is ON). The value stored on C_{L1} propagates to the output through the slave stage which acts as an inverter.

Pulse Register:

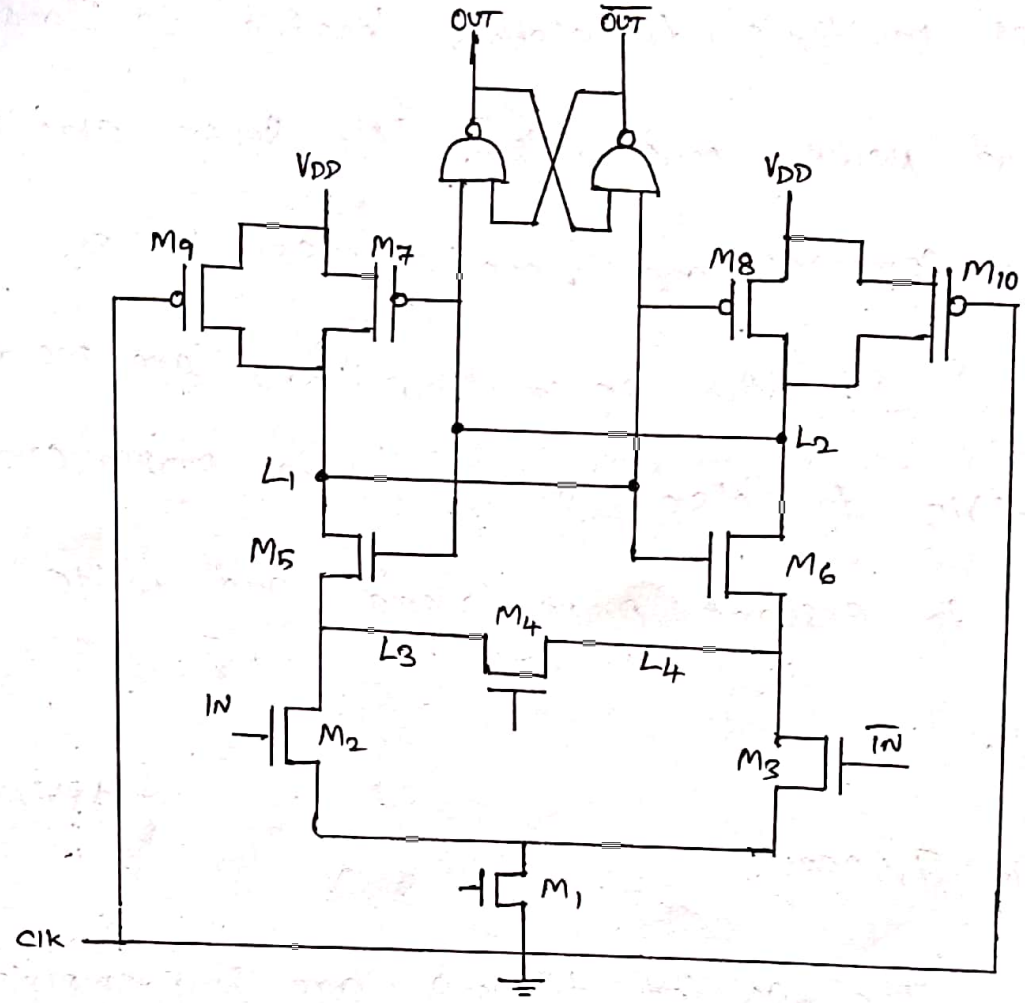
The main idea of pulse register is to construct a short pulse around the rising or falling edge of the clock. This pulse acts as a clock input to a latch.

Pipelining:

Pipelining is a technique of diving the execution of complex digital circuits into smaller sequential stages.

Here, a complex digital circuit is divided into multiple sequential stages and each stage performs a specific operation and passes it to the next stage. The output of one stage becomes the input of the next stage and each stage operates on a different subset of the data.

Sense Amplifier Based Register:



The sense amplifier based register is commonly employed in memory cells, register files and other storage elements in VLSI. The primary purpose of sense amplifier based register is to improve the read and write performance of the memory cell.

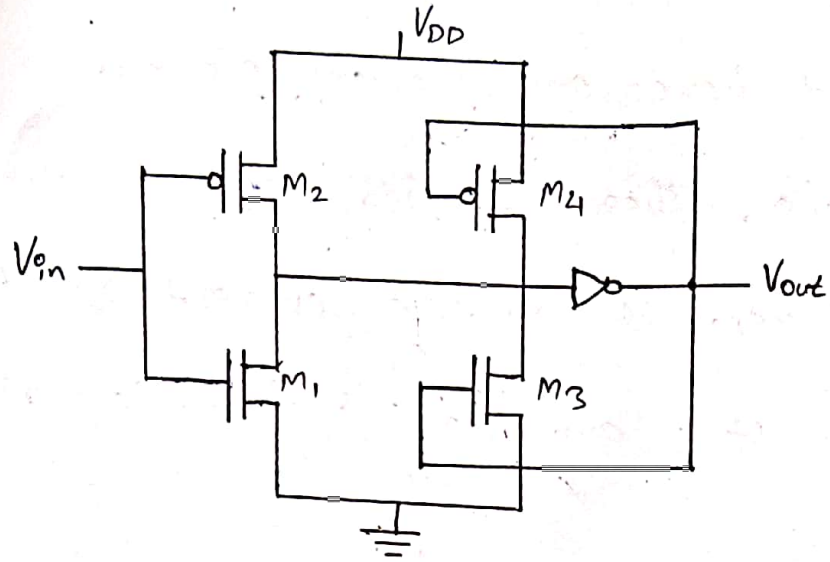
The conventional flip-flops or latches requires multiple transistors leading to larger area and power consumption. The sense amplifier is more compact and needs lesser power.

But the sense amplifiers are more susceptible to noise and requires proper control circuitry to ensured proper read and write operations.

Schmitt Trigger:

The Schmitt triggers are implemented using transistors and other semiconductor devices. The 2 important properties of a schmitt trigger are:

1. It responds slowly to a changing input waveform with a fast transition time at the output.



2. The voltage transfer characteristics of the device displays different switching thresholds for +ve and -ve input signals.

Working:

To turn ~~on~~ a CMOS inverter into a schmitt trigger, hysteresis is introduced by adding positive feedback. The positive feedback provided by the additional PMOS and NMOS creates two threshold levels.

Non-bistable Sequential Circuits:

The non-bistable sequential circuits also known as combinational circuits are digital circuits.

that do not have any memory elements or feedback loops. These circuits produce an output that solely depends on the current input values and do not store any past information about the inputs.

Monostable sequential circuit:

The monostable sequential circuit is also called as one shot or pulse generator. It is a type of sequential circuit that has a single stable state and one unstable state.

The monostable circuits remain in their stable state until triggered by an external input

Astable sequential circuits:

The astable sequential circuits continuosly switches between two unstable states without any external control. Hence it generates continuous square wave or pulse train.

When power is applied, it starts to oscillate between its two unstable states, creating a periodic output waveform.

Timing classification of Digital Systems:

In general, the digital systems can be classified based on their timing behaviour into 3 main categories as:

1. Synchronous
2. Asynchronous
3. Mixed-timing systems.

Clock skew:

The clock skew refers to the difference in arrival time of a clock signal at various elements within a digital system.

In a synchronous digital system, all the components are driven by a common clock signal. But due to routing lengths, & temperature variations,

the clock signal may not arrive simultaneously at all parts of the circuit.

Sources of clock skew:

The clock skew sources can be classified as:

1. Systematic
2. Random
3. Drift
4. Jitter.

Systematic:

Systematic clock skew is that portion which exists even under nominal conditions.

Random:

Random skew is caused by manufacturing variation which affects wire width, thickness and spacing.

Drift:

Drift skew is caused by environmental

variations which occurs very slowly.

Jitter:

Jitter skew is caused by high frequency environmental variations, particularly power supply noise.

Logical clock:

A logical clock is a signal with no clock skew. It produces ideal signals with no skew used by logic designer when describing a HDL.

Single phase clock:

The single phase clock or traditional clock is a single edge clock that alternates between two states in a regular pattern.

The clock frequency is determined by the time period between rising or falling edges of consecutive signals.

Two-phase clock:

The two phase clock has 2 seperate non-overlapping clock signals. During 1st clock, all the even numbered operations are performed and odd are held stable and vice-versa.

Synchronous and Asynchronous Design.

The sequential circuits are classified as asynchronous and synchronous based on the timing of their signals.

Asynchronous Sequential Circuit:

1. Output depends on the sequence in which input signals change.
2. Output will get affected whenever the input changes
3. Difficult to design.
4. Time delay devices are used as memory elements.

Synchronous Sequential circuits:

1. The change of state occurs only in response to a synchronizing clock pulse.
2. Speed of operation depends on maximum allowed clock frequency.
3. Clocked flip-flops are used as memory elements.
4. Comparatively simpler design.

Finite State Machine (FSM):

The finite state Machine (FSM) is a type of sequential circuit which is designed to sequence through specific patterns of finite states in a predetermined sequential manner.

Hazards:

Hazards refers to glitches. Those are unwanted switching transients at the output. It is a temporary false-output value in combinational circuit.

Self-timed Circuit Design:

Self-timed circuit design is a digital circuit design methodology where the circuit operate without a central clock signal.

Instead of using a global clock to synchronize all the circuit elements, self-timed circuits use local control signals to allow each component to operate independently and respond to changes in data or input signals.

This approach offers several advantages including reduced power consumption, improved immunity.

The self timed circuits use the handshaking protocols to control the data flow between the circuit elements.

Benefits of self-timed circuits:

The benefits of self-timed circuit design in VLSI are:

1. Reduced clock distribution complexity
2. Improved performance
3. Lower power consumption
4.

Disadvantages:

1. Design complexity
2. Limited tool support
3. Requires additional circuit control and handshake components.

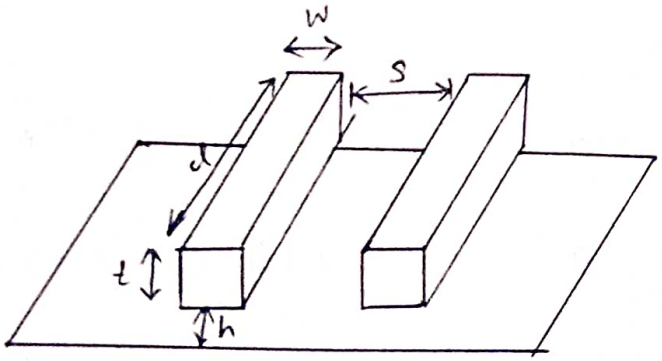
UNIT - 4

INTERCONNECT, MEMORY ARCHITECTURE AND ARITHMETIC CIRCUITS.

Interconnects:

The interconnects play a crucial role in connecting various components on a chip such as transistors, logic gates, memory cells and other functional blocks.

Efficient interconnect design is essential to achieve high performance and low power consumption in modern IC.



w - width
l - length
t - thickness
s - spacing
h - height

$$\text{Pitch} = w + s$$

$$\text{Aspect ratio} = \frac{t}{w}$$

Some of the key parameters that are considered in VLSI interconnect design includes:

1. Resistance (R):

As interconnect length increases, its resistance also increases, leading to voltage drops and signal degradation. To minimize resistance, wider and shorter interconnects are preferred.

2. Capacitance (C):

Capacitance is the ability of the interconnect to store charge. It causes delays during charging and discharging, affecting the overall performance of the circuit.

Capacitance increases with the area and proximity of the adjacent interconnects. So, reducing the width or increasing the spacing between interconnects can help mitigate capacitance effects.

3. Delay:

Delay is the time taken for a signal to propagate through an interconnect. It is influenced by both resistance and capacitance and is a critical factor in determining the speed of the circuit.

4. Metal Layers:

The number of metal layers and their widths impact the routing density and total wirelength., which inturn affects the overall chip performance and area.

5. Pitch:

The pitch is the distance between adjacent metal lines on the same layer.

6. Aspect ratio:

The aspect ratio is the ratio of the height to the width of Interconnect. A higher aspect ratio leads to increased resistance.

7. Cross talk:

Crosstalk is the unwanted coupling of signals between adjacent interconnect. It can cause integrity issues and affects the performance of the circuit.

Electrical wire Models:

The electrical wire models are used to represent the behaviour of metal interconnects that connect various components on an IC chip.

These models help designers analyze and predict the performance of interconnects.

The choice of the electrical wire model depends on the level of accuracy required for specific design and the complexity of the interconnect network.

Sequential Digital circuits:

The sequential digital circuits are a type of circuits whose output is based on both current input and the previous states.

Designing sequential circuits requires careful considerations of timing, state transitions and synchronous design techniques.

General Design Considerations:

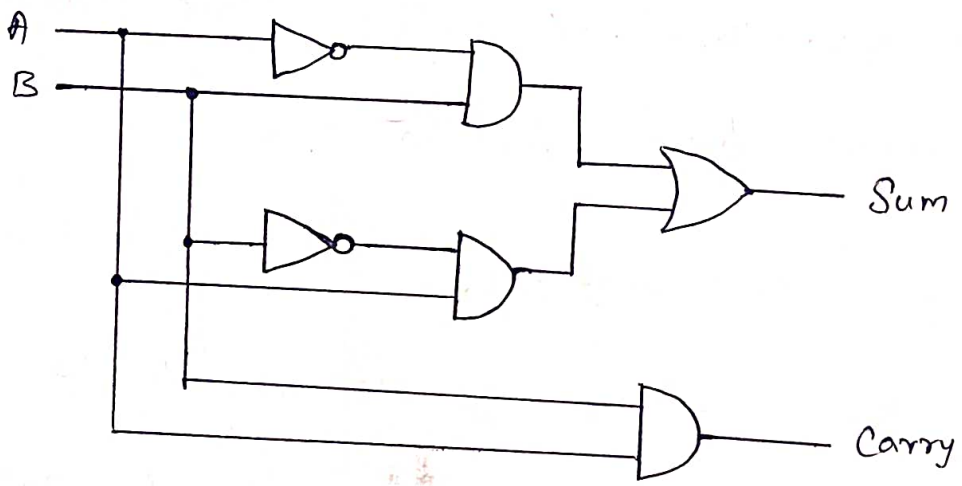
The following aspects are to be kept in mind while designing the sequential digital circuits:

1. Higher reliability
2. Lower power dissipation
3. Lesser cost
4. Improved repeatability
5. Better performance

Adders:

A circuit that adds two bits is called as half adder. A full adder is one that adds three bits.

Half adder:



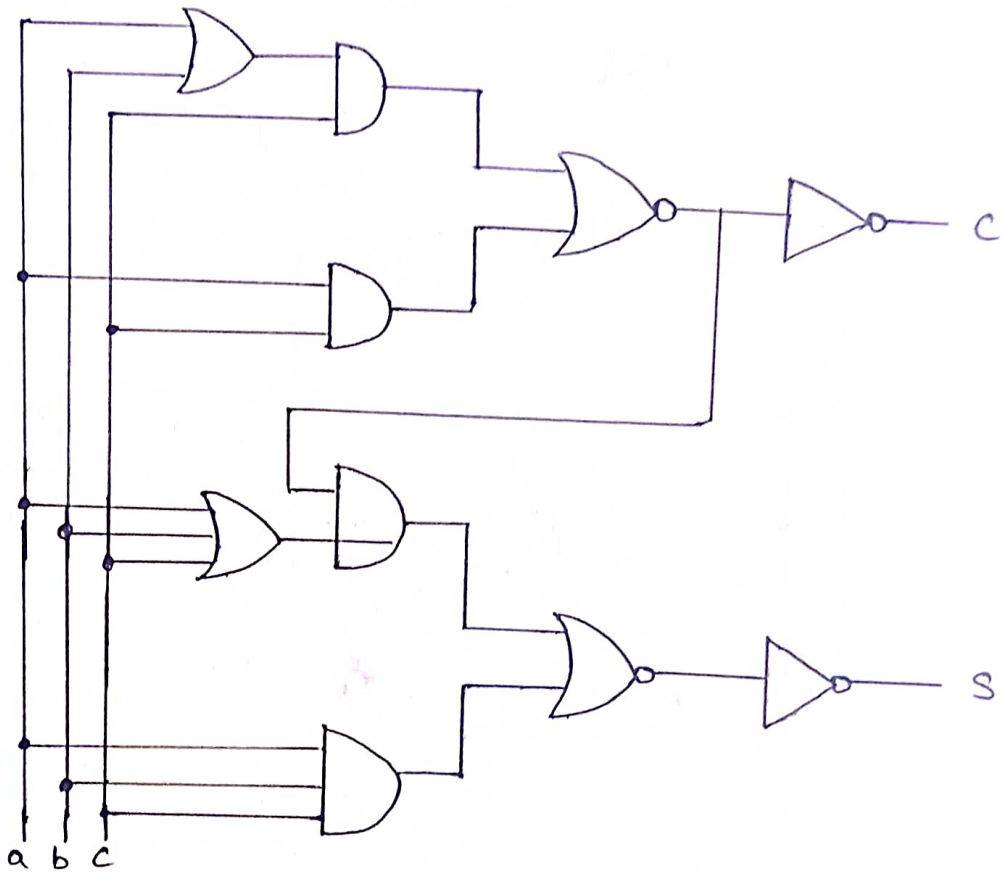
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S = A \oplus B = A'B + AB'$

$C = AB$

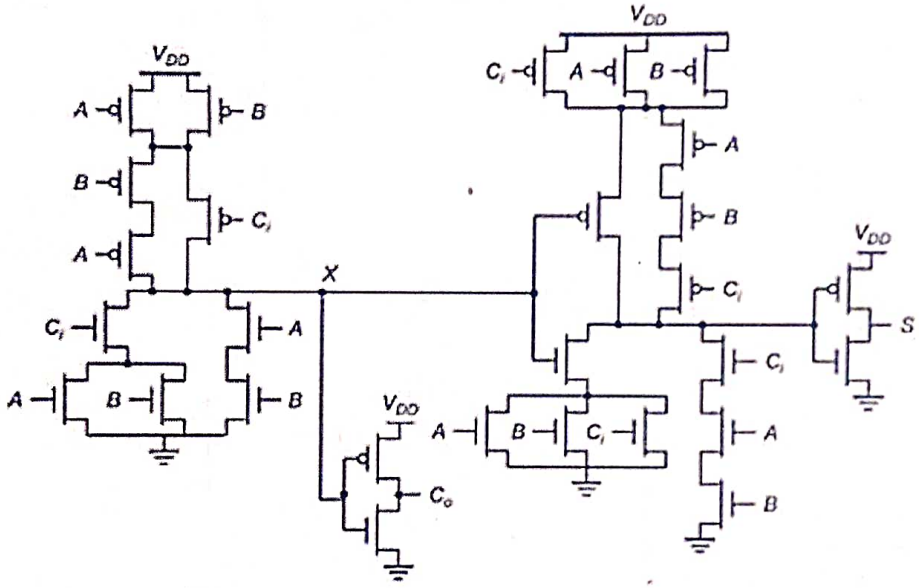
Full adder:

A full adder is a combinational circuit that performs the arithmetic sums of 3 bits.



a	b	c	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The above mentioned full adder can be constructed using the pmos and nmos transistors also which can be implemented on VLSI. This alternative implementation needs 28 transistors which looks like this,



Here,

Sum = $a \oplus b \oplus c$

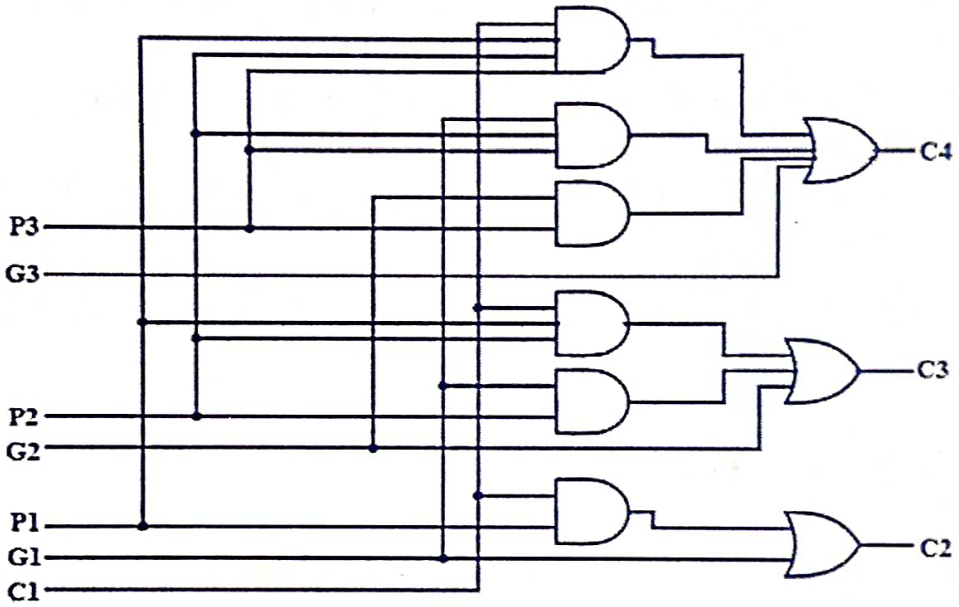
Carry = $ab + c(a \oplus b)$

Ripple carry adder:

The basic principle of a ripple carry adder is to add two binary numbers bit by bit,

Starting from LSB to the MSB. Each stage consists of a full adder, which takes 3 inputs. It produces 2 outputs, the sum and carry, which is propagated to the next stage.

Carry Look-Ahead adders:



While the ripple carry adders are simple to implement, they are generally avoided in high speed or high performance circuits.

In such cases, the ~~to~~ carry look ahead adders are prefered due to the reduced propagation delays and improved performance.

The carry look ahead adder uses the parallel carry computation technique to overcome the propagation delay.

The carry look ahead adder reduces the dependency on carry propagation from one stage to another, resulting in faster addition of numbers compared to ripple carry adder.

One of the key advantages of this adder is that it has constant time delay.

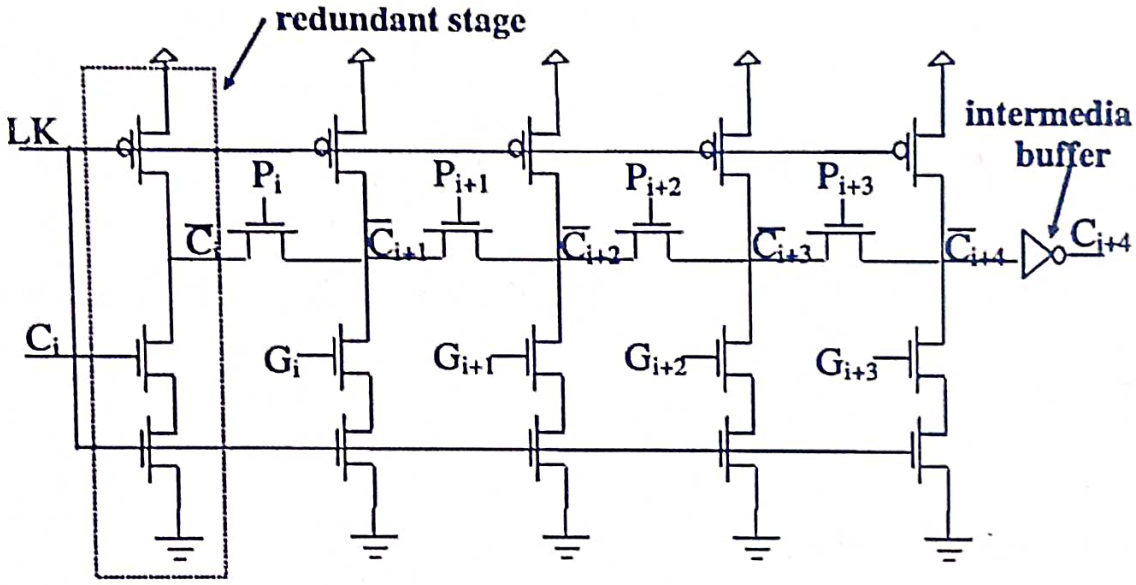
Carry skip adder:

The carry skip adder or carry bypass adder combines the advantages of both ripple carry adder and carry look ahead adder to provide a good trade-off between the speed and area efficiency.

This method divides the ~~carry skip~~ adder into several small blocks each with its

ction carry look-ahead logic. This allows the adder to perform multiple carry computations in parallel and then select the correct carry value based on the final sum.

Manchester Carry-chain Adder:



The manchester carry chain adder ~~is~~ uses a unique approach to generate carry signals. It uses a chain of XOR gates that are used to propagate carry signals from one block of bits to the next..

This faster propagation of carry signa reduces the overall propagation delay of the adder. However, this uses more area when compared to the other adder making the choice difficult for the designers.

Multipliers:

There are several types of multipliers in VLSI circuits, each with its advantages and applications.

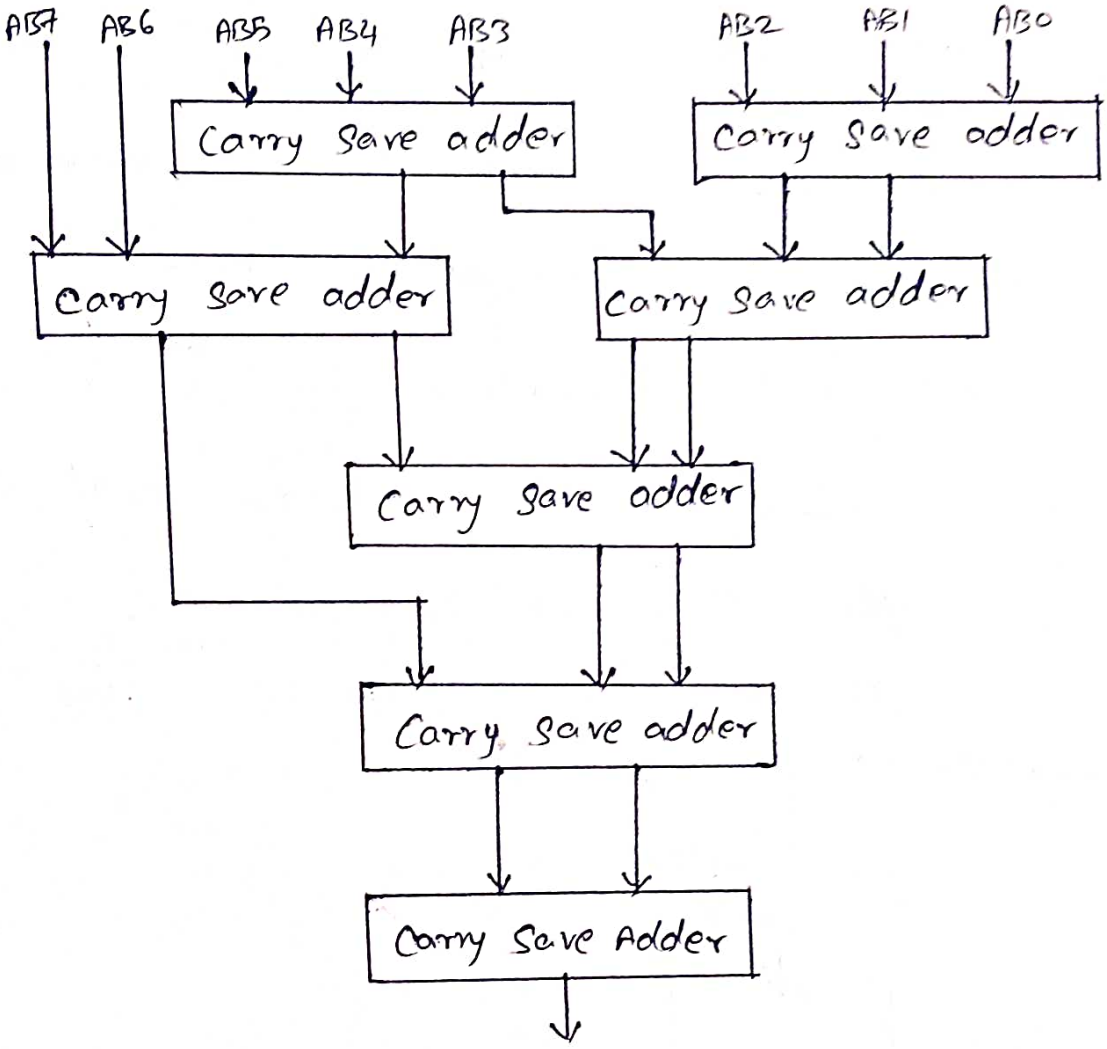
Binary multiplier:

It is a simplest form of a multiplier which performs the multiplication using the basic arithmetic and logic gates.

Wallace Tree multiplier:

The wallace tree multiplier uses a tree based structure to generate partial products in parallel

parallel, reducing the number of adders required. This leads to better speed and area efficiency for moderate bit width multiplication.



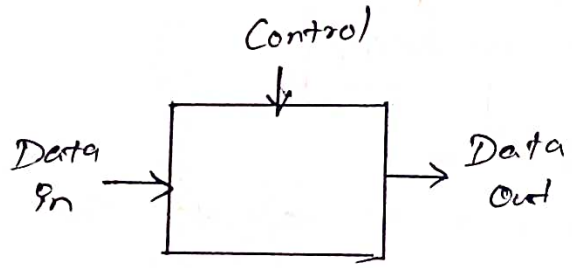
Here, AB0 to AB7 represents the partial products. The wallace multipliers consists of AND gates, carry save adders and carry propagate adder. Here, all the partial products are added at the same time instead of adding one at a time.

Comparator:

The comparator is a circuit which is used to compare the magnitude of two binary numbers.

The basic operation of a comparator involves comparing the corresponding bits of two binary numbers and generating output to indicate whether one number is greater than, equal to or less than the other number.

Shift Registers:

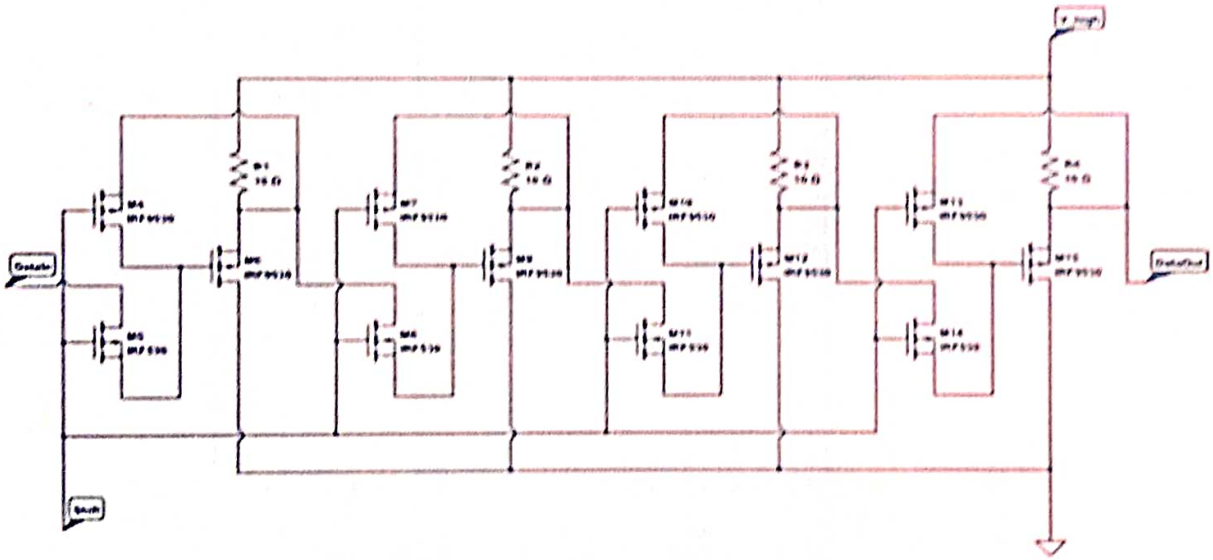


The shift registers are used to shift the data or word to left or right over the position desired by the user.

Barrel Shifter:

A barrel shifter has n-data inputs, n-data outputs and a set of control input that specify how to shift the data between input and output.

The various shift operations that can

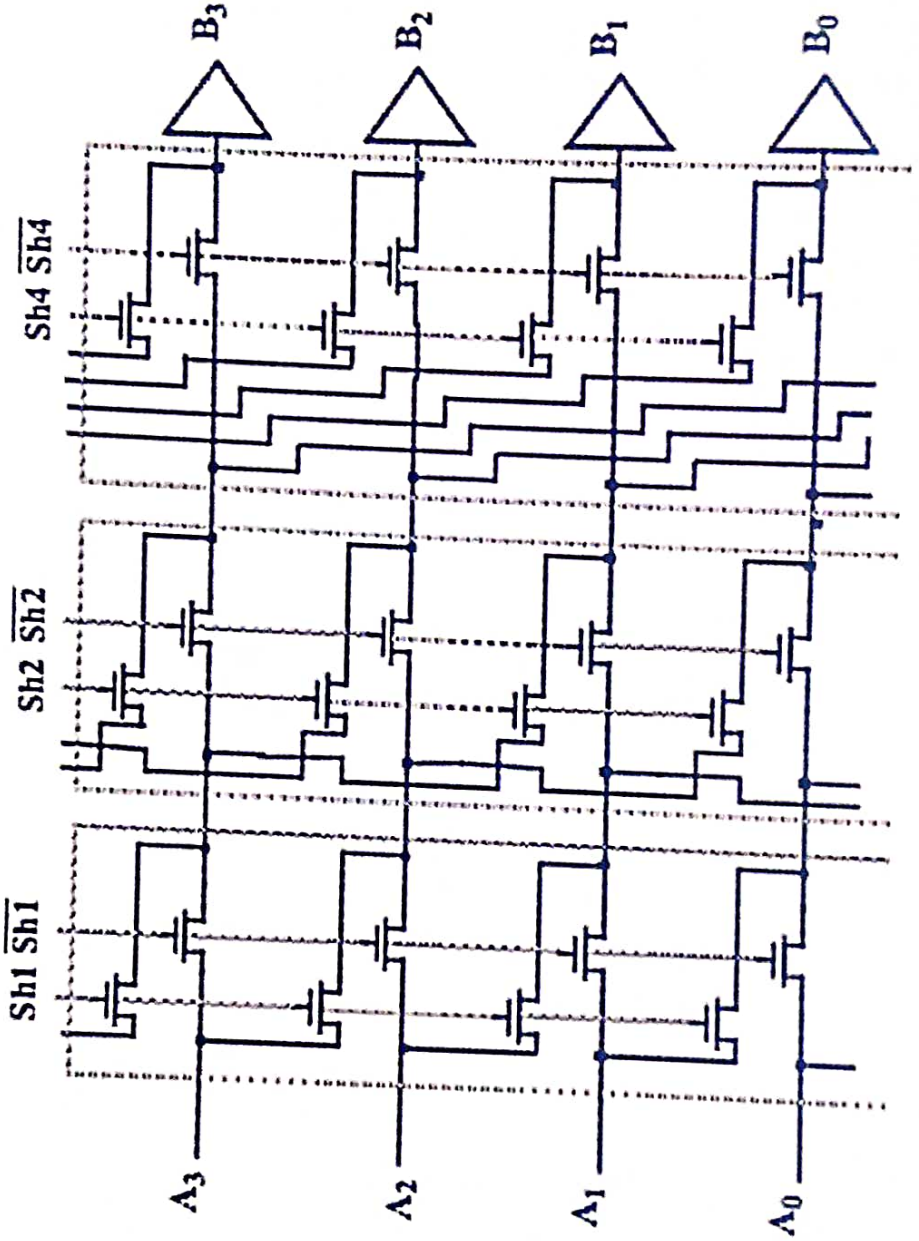


be performed in shift registers are:

1. Logical right shift
2. Left shift
3. Arithmetic right shift
4. Arithmetic left shift
5. Rotate.

Logarithmic Shifter:

In this, the speed of the n-bit shifter is proportional to log(n)



Hence it can provide faster shifting operations. It uses stages of multiplexers which decompose the shift into power of two stages.

The barrel shifter is better for small shifters and the log shifter is preferred for the larger shifters both due to size and delay.

Logic Implementation using Programmable Devices:

The programable logic devices (PLD) are the standard ICs that can be programmed to implement the desired functions. The important features of PLD are:

1. No customized mask layers
2. fast design turnaround
3. A single large block of programmable interconnect
4. A matrix of logic macro cells.

The different types of PLDs are read-only memory (ROM), Programmable array logic (PAL) and programmable Logic array (PLA).

Read-only Memory (Rom):

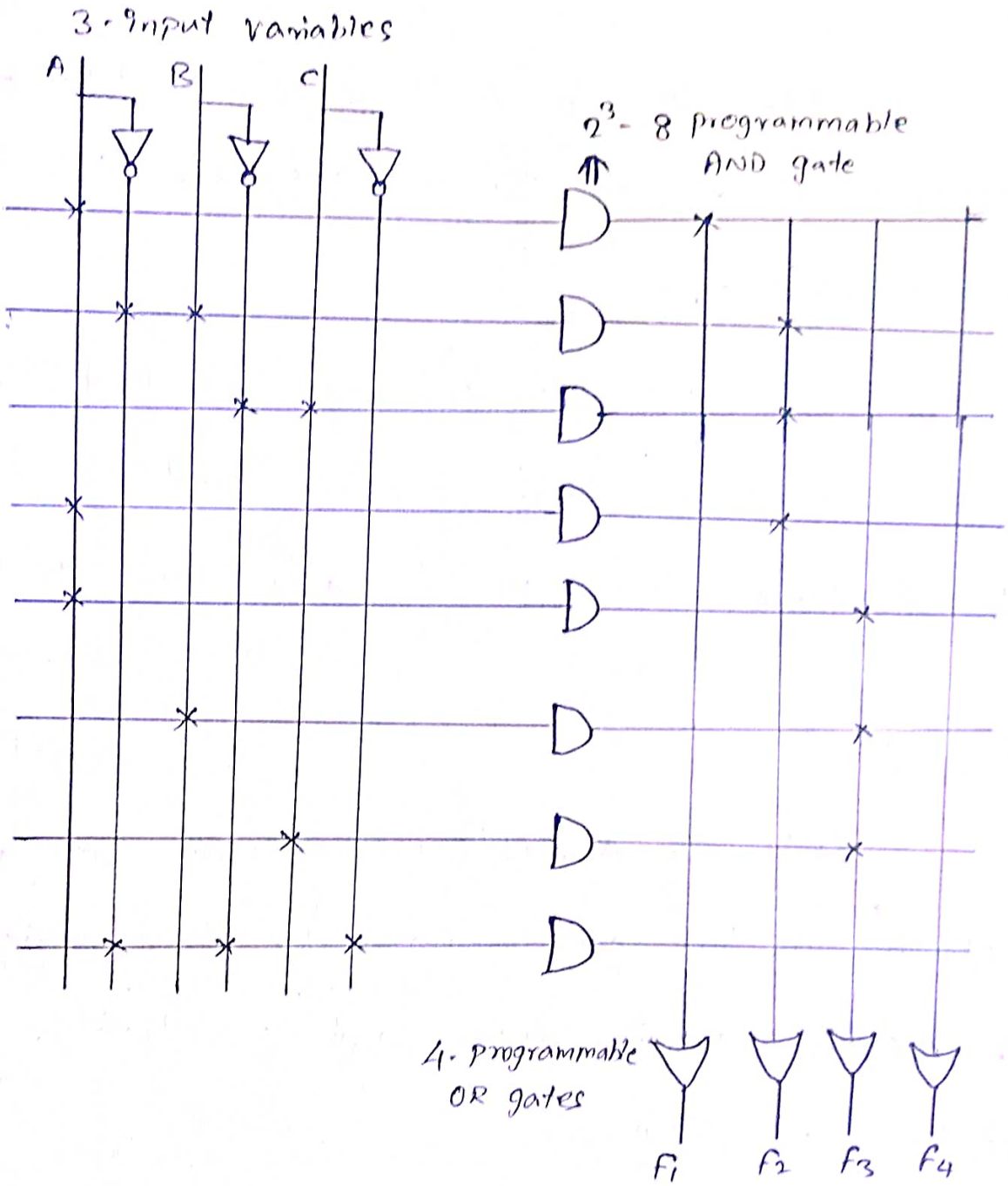
The Rom is the simplest type of programmable ~~ar~~ Ic which can be used to once to store binary data.

The most commonly used types of Ro... use a metal fuse that can be blown permanently (prom... An electrically programmable Rom or EPROM uses a programmable mos transistors whose characteristics are altered by applying a high voltage.

A masked Rom is a regular array of transistors permanently programmed using custom mask patterns.

Programmable Logic Array (PLA):

A PLA is similar to a Rom. In PLA, a set of programmable AND and OR planes are there. They both are programmable and used to implement combinational logic circuits.



A PLA has 2^N AND gates for N input variables and M OR gates for M ~~inpu~~ outputs, each of which can be programmed to generate a product term of input variables.

A size of PLA is specified by the number of inputs, no. of product terms & outputs.

PLA can be mask-programmable or field programmable. The PLA reduces the chip area and it is flexible.

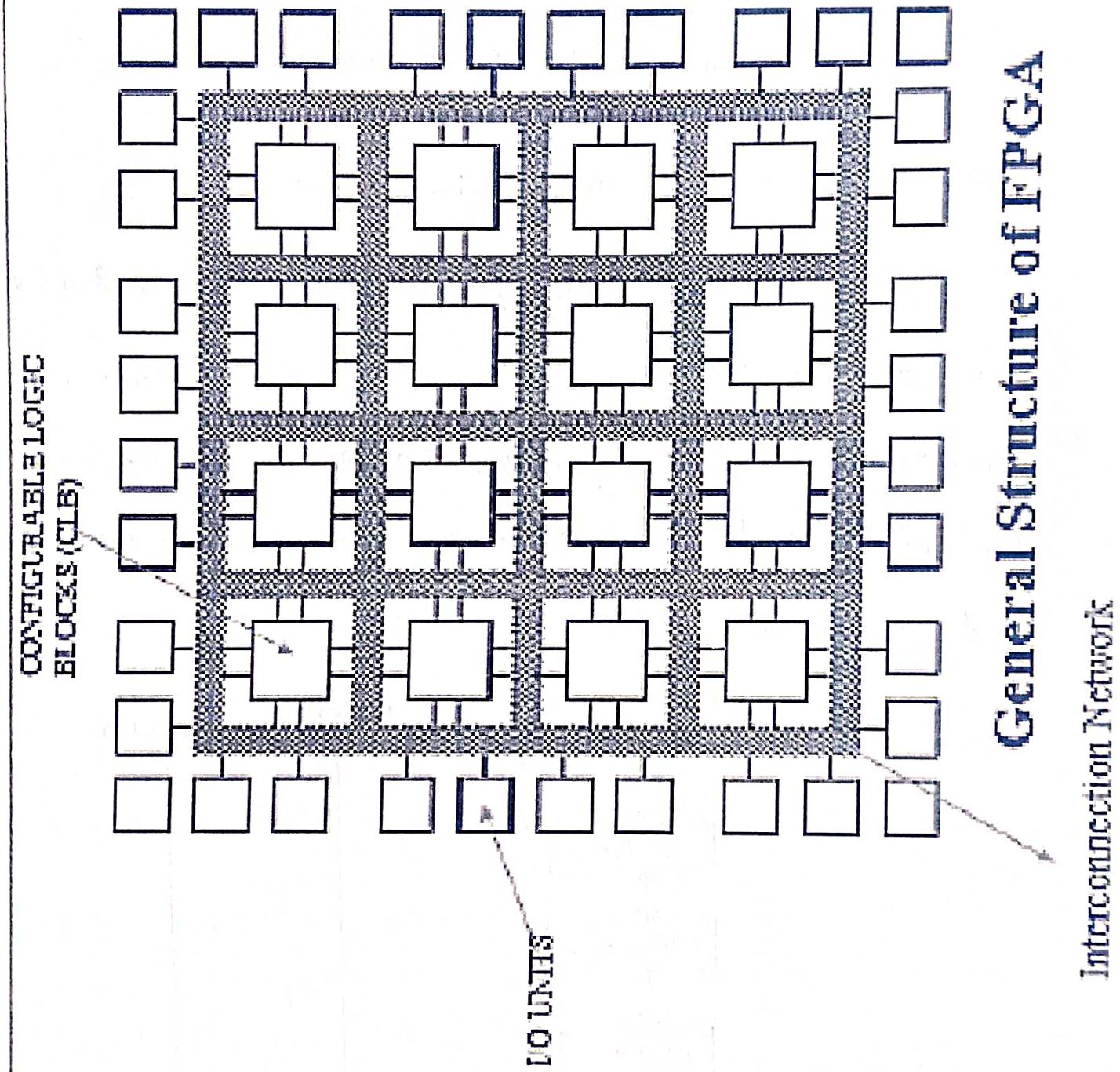
The disadvantage of PLA is that its propagation delay is more and it is limited to functions that can be expressed in SOP form.

FPGA:

FPGA is a field programmable Gate Array. It is a type of programmable logic device used in digital circuit design and prototyping. The key features of FPGA are:

1. Configurability
2. Look up table
3. Programmable interconnect
4. High parallelism
5. Partial reconfiguration
6. HDL Implementation

General Structure of FPGA:



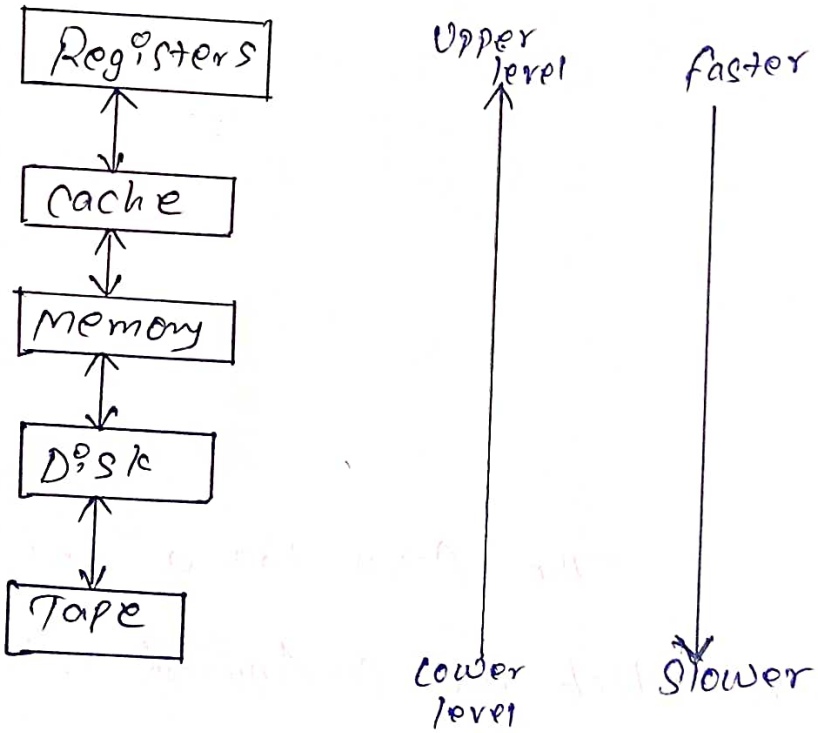
The FPGA has a set of input & output blocks which are configured as fixed i/p, & output.

The basic architecture of FPGA consists of:

1. Configurable Logic Block (CLB)
2. I/O block
3. Programmable interconnect.

Memory Architecture and Building Blocks:

The memory architecture refers to the organization and hierarchy of memory components in a computer system. It defines how data and instructions are stored, accessed and managed within the system.



The data storage devices of various sizes are required for most IC designs. A collection of storage cells together with associated circuits are needed to transfer information in and out of the device.

Memory element terminology:

Latch:

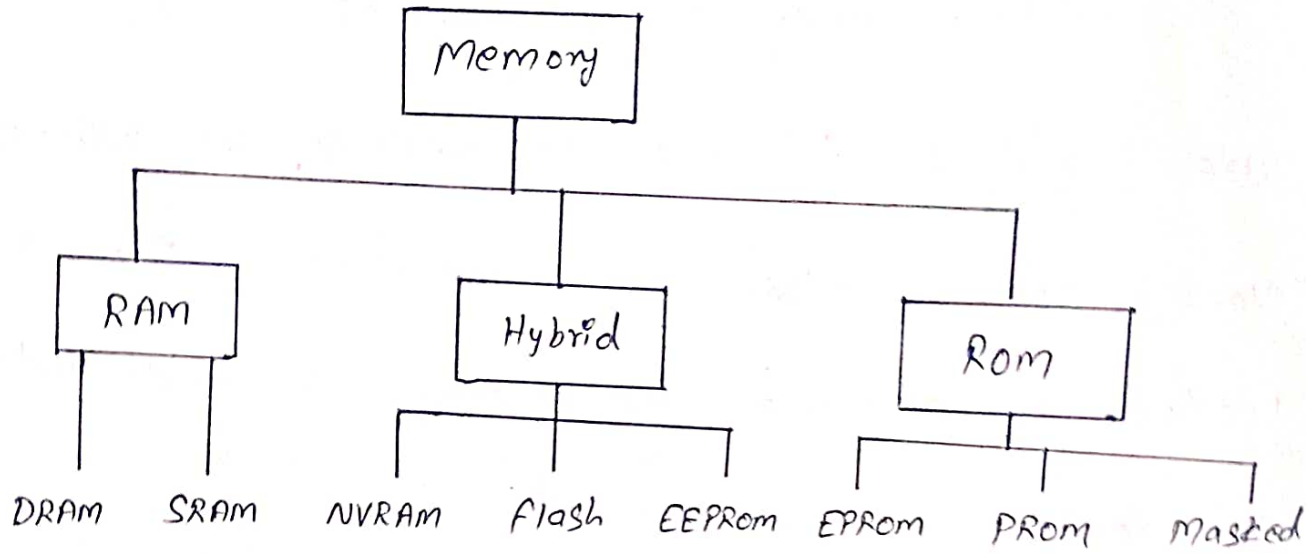
Latches are transparent while the internal memory is being set from input data.

flip-flop:

The flip-flops are not transparent - reading input value and changing its output are seperate events.

Types of memory:

Many types of memory devices are available for use in modern computer system.



The Random Access memory is a memory array with individual bit access and has both read and write capabilities.

The read only memory has no write capabilities.

Flash Memory:

. The entire content in the flash memory can be erased by less than a second. The erasing process is done by an electric pulse and hence it is also called flash EEPROM. It is a non-volatile memory.

Type	Volatile	Writeable	Erase size	Max Erase cycles	cost (per byte)	Speed
SRAM	Yes	Yes	Byte	Unlimited	Expensive	fast
DRAM	Yes	Yes	Byte	Unlimited	Moderate	Moderate
Masked Rom	No	No	N/A	N/A	Inexpensive	fast
PROM	No	Once	N/A	N/A	Moderate	fast
EPROM	No	Yes	Entire chip	Limited	Moderate	fast
EEPROM	No	Yes	Byte	Limited	Expensive	Read - fast write - slow
Flash	No	Yes	Sector	Limited	Moderate	Read - fast write - slow

Comparison of various Memory elements

These building blocks work together to form the memory systems with different capacities, access times and functionalities.

UNIT - 5

ASIC DESIGN AND TESTING

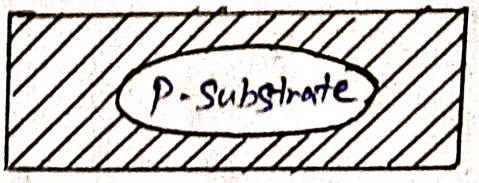
Introduction to wafer to chip fabrication process.

The Ic fabrication is a sequential and a lengthy process. The various steps involved in Ic fabrication process are:

1. Wafer preparation
2. Oxidation
3. Diffusion
4. Ion implantation
5. Chemical vapour deposition
6. Metalization
7. Phoblithography
8. Packaging

Step - 1:

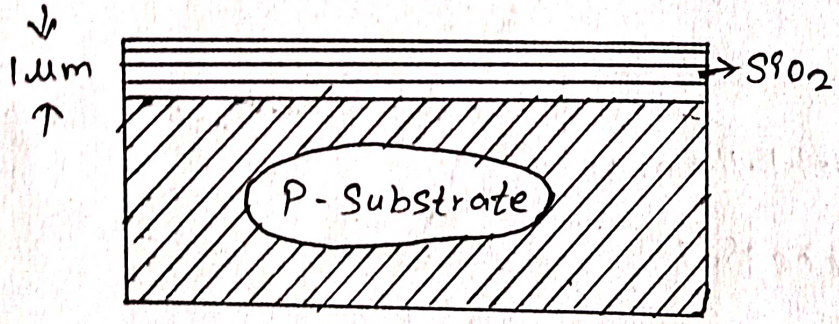
Processing is done on a thin film of pure silicon crystal. P-impurities are introduced as crystal.



The typical wafer diameter is 75 to 150 m and thickness is 0.4 mm. The impurity is boron having concentrations of $10^{15}/cm^3$ to $10^{16}/cm^3$ giving resistivity of 25 Ω-cm to 2 Ω-cm.

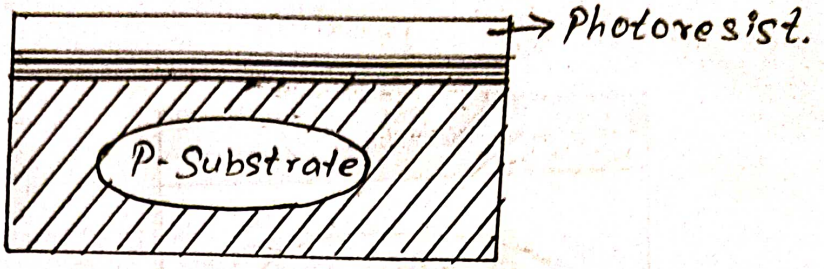
Step. 2:

A layer of silicon dioxide (SiO_2) is grown over the surface of wafer for protection of surface. The thickness of SiO_2 is 1 μm.



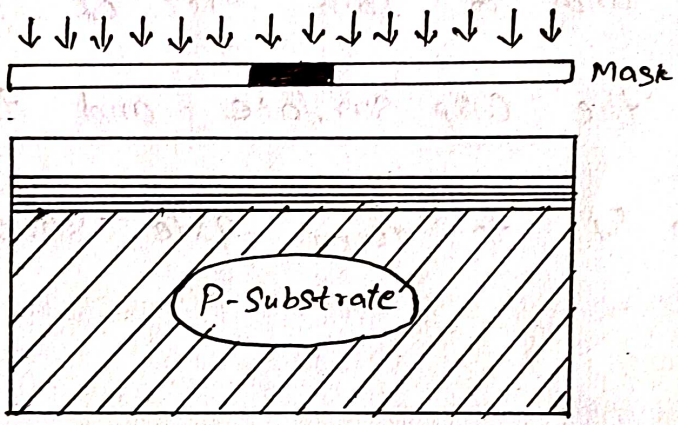
This layer acts as barrier to dopants during processing.

Step-3:



The SiO_2 layer is now covered with photo resist which is deposited on wafer.

Step 4:

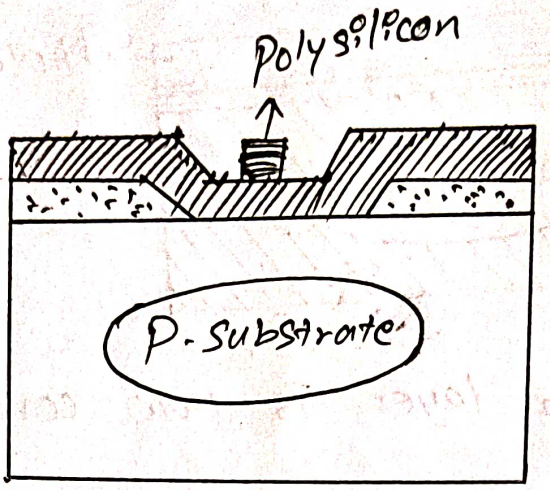


The photoresist layer is exposed to UV light through a mask. The mask corresponds to regions onto which diffusion takes place.

Step-5:

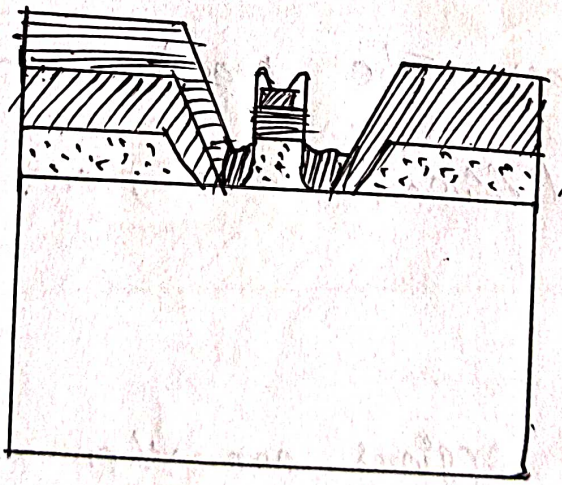
These regions are then etched together so that wafer is exposed in window defined by mask.

Step 6:



The photoresist layer remains on substrat is removed and a thin layer of SiO_2 (0.1 μm) is grown over the chip surface and then polysilicon is deposited on it to form gate structure.

Step 7:



The diffusion is acheived by heating the wafer to high temperature and passing n-type impurity

over the surface. The SiO_2 layer is grown and masked with photoresist and then etched to expose specific areas of polysilicon. The wafer is then metal deposited over its surface to a thickness of 1μm. The metal is usually aluminium.

Microchip Design Process:

Oxidation:

During the process of IC fabrication when silicon is exposed to oxygen or water vapour at high temperature to form a continuous layer of SiO_2 is called as thermal or wet oxidation.

$$Si + O_2 \rightarrow SiO_2$$

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

Lithography:

Lithography is a process of transferring patterns of geometric shapes in a mask to a layer

of radiation sensitive material for covering surface of semiconductor wafer.

Diffusion:

The process of introducing controlled amounts of dopants into semiconductors is called diffusion. It is carried out in furnace where inert gas containing dopant is pass through the wafer at temperature range 800 to 1200°c.

Ion Implantation:

The process of introducing high energy charged particles into the substrate is called as ion implantation.

Metallization:

Metallization is a process of formation of metal films for interconnections, ohmic contacts and rectifying metal semiconductor contacts.

Issues in test and verification of complex chips:

Some of the major issues includes:

1. Design Complexity:

Complex chips contain millions of transistors and intricate interconnections. As a result, the test and verification process become more difficult.

2. functional verification:

Ensuring that the chip functions correctly according to its specifications is a major challenge.

3. Timing & Synchronization:

As chips become faster, dealing with timing issues and ensuring proper synchronization between different components is challenging.

4. Power constraints:

Testing & ~~verificat~~ verifying a chip adhering

to the power limits require sophisticated power management and optimization techniques.

5. Test Access:

The limited number of test pins can lead to difficulty in observing and controlling internal signals during testing.

6. Security concerns:

Ensuring the chips resistance to attacks like reverse engineering and side channel attacks adds an additional complexity to the verification process.

The automated testing and verification tools help improve the efficiency and coverage of the testing process.

Testing and Logic verification:

The CMOS IC tests can be categorized as:

1. Functionality test
2. Silicon debug
3. Manufacturing test.

The functionality test verifies that the chip performs its intended function. The silicon debug tests helps in finding the manufacturing faults. in silicon area.

The manufacturing tests verify that every transistor, gate and storage elements in the chip functions correctly.

Logic Verification:

Chip functional testing is done by simulation. The chip simulation is usually done at HDL level. The verification engineers write test bench for HDL.

The bug tracking system is an important tool to use during verification. It allows to manage a wide variety of bugs.

Application Specific ICs (ASICs)

Application Specific Integrated circuit is a full-custom circuit in which every mask is defined by the customer or a semi-custom circuit where only few masks are defined.

ASIC is custom designing IC for a particular application such as processing unit of a mobile phone. ASIC is useful for high volume production.

ASICs are commonly used in various industries such as telecommunications & Automotives. The design process of ASIC is complex and costly.

But the benefits of tailored performance and efficiency overweigh the initial investment for certain mission-critical applications

Advantages:

1. Better performance.
2. More secure for design circuit
3. Compact
4. Contains digital as well as analog circuits.

Disadvantages:

1. Cannot be easily replaced if damaged.
2. Costly.

Types of ASICs:

1. Full custom ASIC
2. Semi-custom ASIC

ASIC Design Flow:

ASIC Design flow is a series of steps a methodologies involved in ASIC. It has following key stages:

1. Specification and Architecture
2. Design entry
3. RTL Design
4. Functional verification
5. Synthesis
6. Physical design
7. Design for test
8. Timing closure
9. Tapeout
10. Fabrication and testing
11. Packaging and System

Test Bench:

In the ASIC test bench, the user defines the input stimuli and expected outputs to stimulate

the design under test. The test bench monitors the responses generated by ASIC and compares them to the expected outputs to check for correctness.

The test bench can be written in HDL like verilog or VHDL or in specialized verification languages like system verilog.

Writing the test benches in Verilog HDL:

A test bench allows you to simulate and verify the functionality of your design before moving on the actual hardware implementation.

The procedure to write a test bench using Verilog HDL is:

1. Module declaration
2. Instantiate the DUT (Design Under Test)
3. Define inputs
4. Apply inputs
5. Monitor outputs
6. Simulate & Run
7. Analyse results

A simple example of verilog test bench

for an AND gate:

```
module tb_and_gate;
// declare input and output
signals
    reg a,b;
    wire y;
// Instantiate the design under Test (DUT)
    and_gate and_inst (.a(a), .b(b), .y(y));
//Apply input stimuli initial begin
    $display ("Testing and gate...");
    a=0; b=0; #5;
    a=0; b=1; #5;
    a=1; b=0; #5;
    a=1; b=1; #5;
  $finish;
end
//monitor outputs
 always @(y) $display ("output y = %b", y);
 endmodule
```

Automatic Test Pattern Generation:

Automatic test pattern generation (ATPG) is a process used to automatically create the test patterns that can be used to test the functionality and reliability of IC.

The goal of ATPG is to generate the test patterns that can detect the manufacturing defects. It uses various algorithms to efficiently generate the test patterns ensuring high test coverage fault detection.

Design for Testability:

The design for testability covers three important approaches:

1. Ad-hoc testing
2. Scan based approaches
3. Self and built-in test

Adhoc testing:

The Adhoc testing is a dynamic testing approach where the tester explores the functionality of the design and identifies the potential defects based on their own understanding or intuition.

Adhoc testing can be useful for quickly discovering certain issues like identifying the defects.

Some of the ad hoc testable design techniques are:

1. Partition and Mux technique
2. Initialize Sequential Circuit
3. Disable internal clocks
4. Avoid Asynchronous Logic
5. Avoid delay dependent logic

Ad hoc methods were the first DFT techniques introduced in 1970s. The goal was to target only those portions of circuit that would be difficult to test and add circuitry to improve the controllability and observability.

Scan Design:

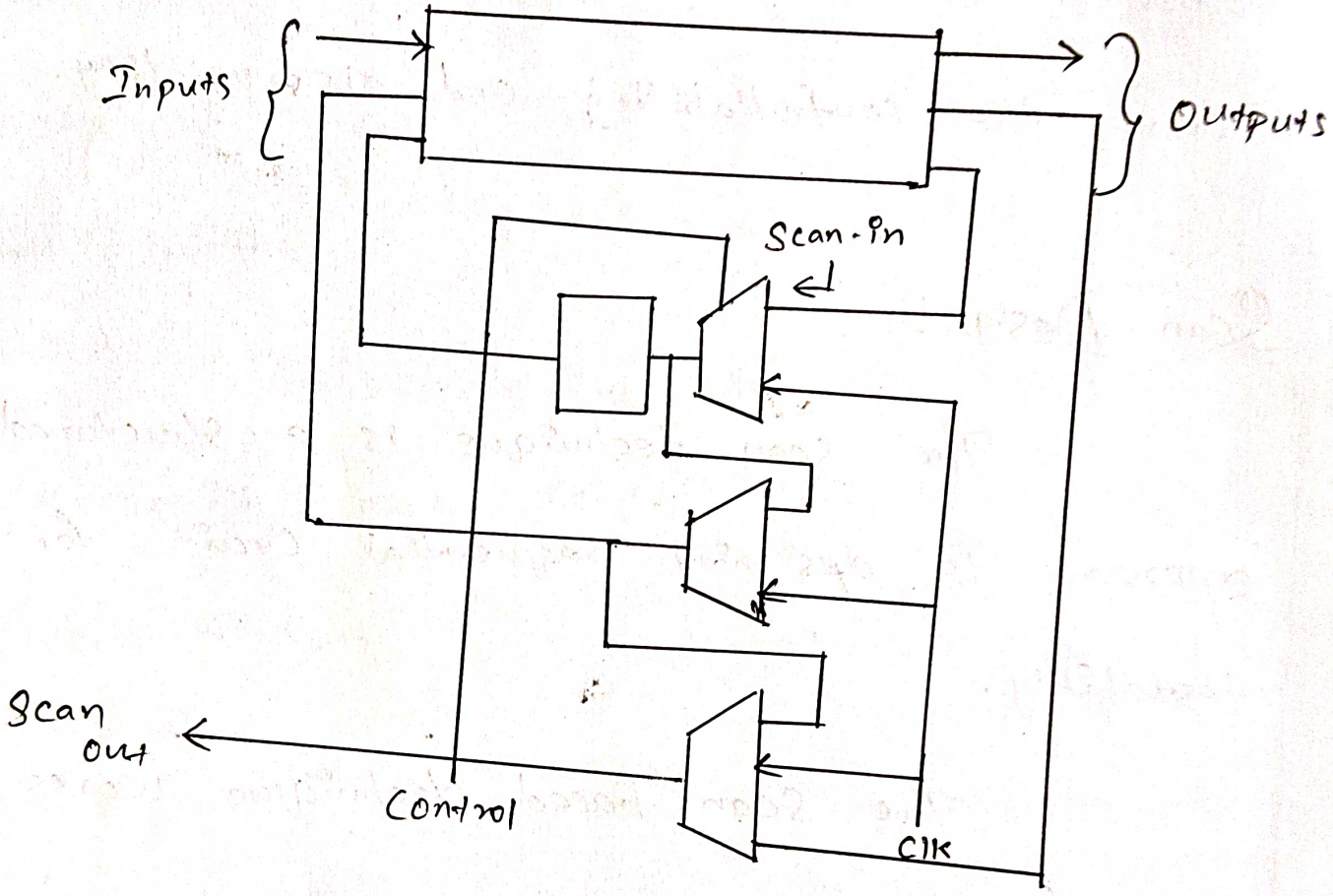
The scan technique is a structured approach to designing sequential circuit for testability.

The scan based technique works in two modes:

1. Test mode
2. Normal mode

In test mode, the scan-in signal is clocked into scan path and output of last stage is scanned out.

In normal mode, the scan in ... disabled and the circuit functions as ... sequential circuit.

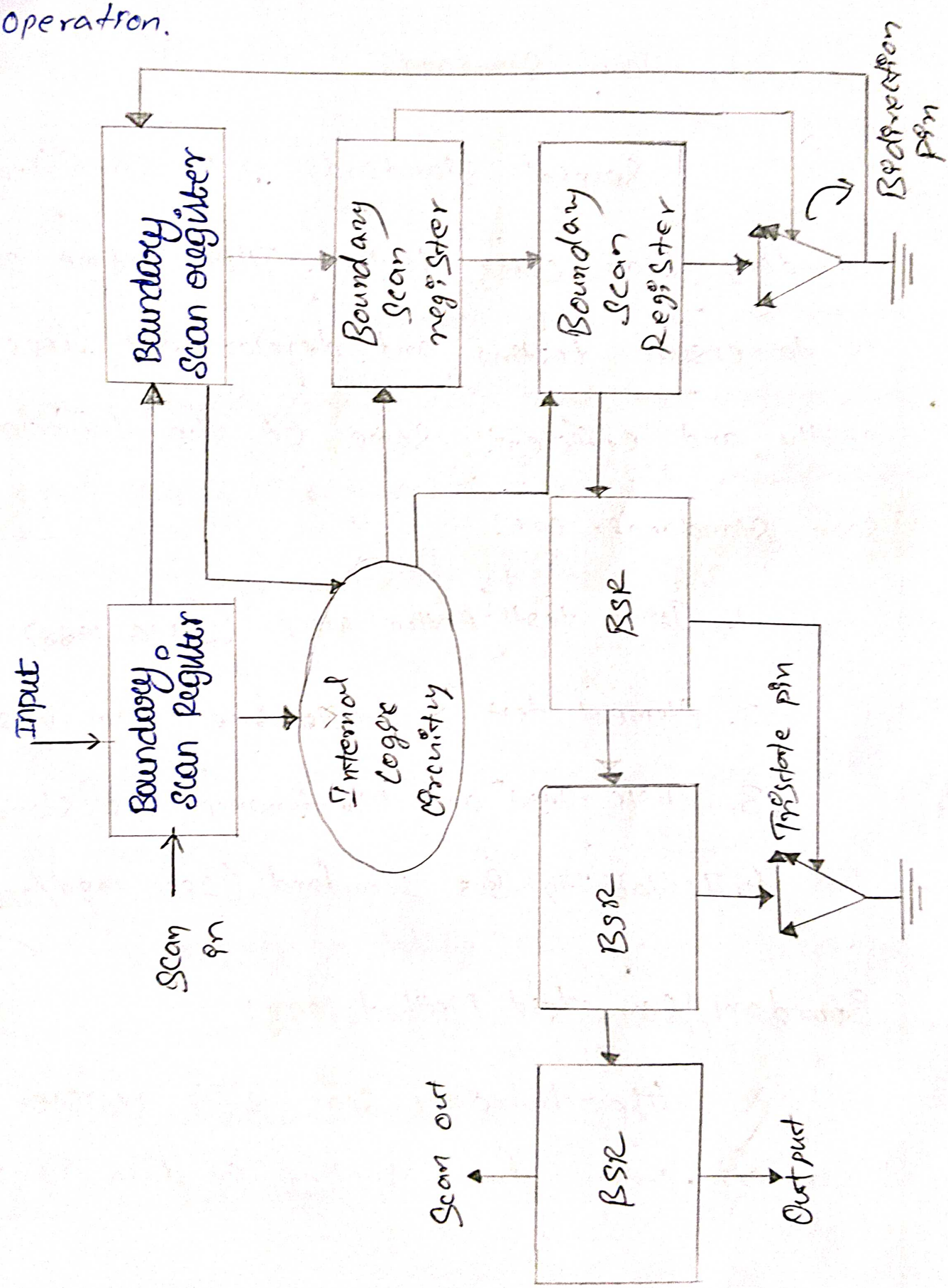


Boundary Scan Check:

Boundary scan check has the following advantages over other testing methods:

1. Increased fault coverage
2. Time efficient.

through the shift register during the scan operation.



3. Simple

4. Accurate and efficient.

Boundary Scan Standards:

Several standards are specified for boundary scan check testing. Their prime objective is to ensure testing and development less costly and efficient. Some of the boundary scan standards are:

1. Joint test Action group (JTAG 1988)
2. Element test & maintenance (ETM VHSIC)
3. VHSIC Test and Maintenance Bus standard
4. Testability Bus standard (IEEE 1989/IEEE 1149.1)

Boundary Scan test Methodology:

The boundary scan shift register prevents output from rippling as data is shifted

The test set is scanned into boundary scan register (BSR) by using a scan in port with test stimuli input. The response of the circuit is captured in parallel by BSRs in series and scanned out through scan out port.

The boundary scan path is having serial input output cells and has appropriate clock pads. The cells or pads are provided for:

1. Interconnections between chips
2. Internal self test

The various tests that are carried out by the architecture IEEE 1149 are:

a) Sampling & setting chip input and outputs

b) Connectivity between test components

c) Distribution and collection of self test and build in test results

Built-in self Test (BIST)

The BIST is used to verify the functionality and integrity without relying the external test equipments. It involves incorporate specific test circuits within the system to perform self diagnostic checks.

The advantages of BIST are:

1. Low cost
2. High quality testing
3. Faster fault detection
4. Ease of diagnostics
5. Reduced maintenance & repair costs

The essential modules required for BIST are:

1. Pseudo random pattern Generator
2. Output response Analyser.

IDDQ Testing:

IDDQ testing is used to identify the defects in Ic by measuring the quiescent supply current when the circuit is in a stable state with no inputs changing.

During this test, the Ic is placed in a low power mode, ~~on~~ where it is not actively processing any signals and IDDQ current is measured.

The IDDQ test is performed by applying the test vector and then monitoring the current drawn from the power supply. This test requires more time but fault detection capability is greatly improved.

The design guidelines for IDDQ testability are:

1. Low static current states
2. No active pull-ups / pull-downs
3. No internal drive conflicts
4. No floating nodes
5. No degraded voltages.